

Research Article

Low Power 256-bit Modified Carry Select Adder

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Abstract: Carry Select Adder (CSLA) is one of the high speed adders used in many computational systems to perform fast arithmetic operations. When compared to earlier Ripple Carry Adder and Carry Look Ahead Adder, Regular CSLA (R-CSLA) is observed to provide optimized results in terms of area. This study proposes an efficient method which replaces the RCA using BEC. The modified CSLA architecture has been developed using gate-level modification to significantly reduce the delay and power of the CSLA. Based on this modification 8-, 16-, 32-, 64- and 128-bit Square-Root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design for 256-bit has reduced power and delay as compared with the regular SQRT CSLA. Designs were developed using structural Verilog module and synthesized using Xilinx ISE simulator and the implementation is done in cadence RTL compiler using 0.18 μm technology. For 256-bit addition in this study, it is proposed to simple gate level modification which significantly reduces the power by 19.4% when compared with R-CSLA. The result analysis shows that the proposed architecture achieves two folded advantages in terms of delay and power.

Keywords: BEC, cadence, CSLA

INTRODUCTION

Power and area have major role in the designing of integrated circuit because of the increase in popularity of portable systems as well as the rapid growth of power density in VLSI circuits. Addition usually influences strongly on the overall performance of digital systems and a crucial arithmetic function. Adders are most widely used in electronic applications. For example, in microprocessors, millions of instructions per second are performed. Due to the increase in the portability of the devices like mobile, laptop etc., require more battery backup. Low power (Edison and Manikandababu, 2012) and area efficient addition and multiplication have always been a fundamental requirement of high performance processors and systems. Designing efficient adder is the most difficult problem in VLSI design.

Carry Select Adder are used for high speed application by reducing propagation delay. The basic operation Carry Select Adder (CSLA) is parallel computation. CSLA generates many carries and partial sum. The final sum and carry are selected by multiplexers (mux). Multiple pairs of Ripple Carry Adders (RCA) are used in CSLA (Mitra and Dutta, 2012) structure. Hence, the CSLA is not area efficient.

The proposed method use Binary to Excess-1 Converter (BEC) instead of RCA with $C_{in} = 1$ in the regular CSLA. The main goal of this BEC logic is to use lesser number of logic gate than the n-bit Full

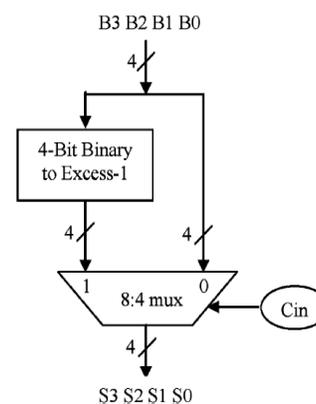


Fig. 1: BEC with mux

Adder. So that, the modified CSLA architecture is lower area and power consumption. In the modified CSLA the input bits are given in linear manner to achieve low power. This study is implemented for higher order bits (till 256 bits) and the Comparison between Regular SQRT CSLA and modified SQRT CSLA is discussed below:

Binary to Excess -1 Converter

The main idea of this study is to use BEC instead of the RCA with $C_{in} = 1$ in order to reduce the area and power consumption of the regular CSLA. To replace

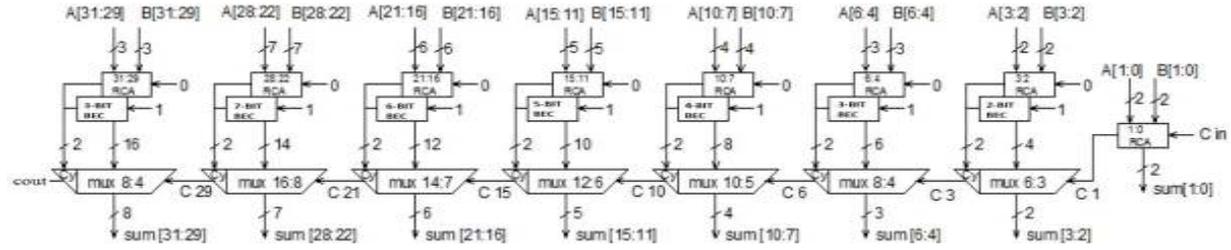


Fig. 2: Modified 32-bit Sqrt CSLA

the n -bit RCA, an $n+1$ -bit BEC is required. The modified CSLA architecture has developed using Binary to Excess-1 Converter (BEC). Figure 1 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. The XOR gate in BEC of Modified CSLA is replaced with the optimized XOR gate in And or Inverter (AOI) of Modified Area Efficient CSLA. With BEC there is reduction of gates by replacing n bit RCA with $n+1$ bit BEC. When the optimized XOR gate is used in Modified CSLA, it is verified that there is large reduction in number of gates. The multiplexer (mux) is used to select either the BEC output or the inputs given directly to a BEC circuit of next block. In this design, the major function of mux is to derive the adder speed.

According to the control signal C in (Subha and Durga, 2013), the mux is used to select the output from the inputs (input bits as per the block size and the BEC output). The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC (Pandey *et al.*, 2013) are listed as (note the functional symbols \sim NOT, $\&$ AND, \wedge XOR):

$$\begin{aligned} X0 &= \sim B0 \\ X1 &= B0 \wedge B1 \\ X2 &= B2 \wedge (B0 \& B1) \\ X3 &= B3 \wedge (B0 \& B1 \& B2) \end{aligned}$$

Regular Sqrt carry select adder: In this part the regular Sqrt CSLA operation and its delay calculation are discussed. A Sqrt carry select adder is constructed using the conventional 4-bit Ripple Carry Adder (RCA). The RCA uses multiple full adders to perform addition operation. Each full adder inputs a carry-in, which is the carry-out of the preceding adder.

The CSLA divides the words to be added into blocks and forms two sums for each block in parallel, one with assumed carry in (C_{in}) of 0 and the other with C_{in} of 1. The carry-out from one stage of 4-bit RCA is used as the select signal for the multiplexer.

This selects the corresponding sum bit from the next block. This speeds up the computation process of the adder. Thus, the carry select adder achieves higher speed of operation at the cost of increased number of devices used in the circuit. This in turn increases the area and power consumed by the circuits of this type of structure.

Table 1: Area count of CSLA

Group no.	Regular	Modified
2	64	50
3	94	73
4	124	96
5	154	119
6	184	142
7	214	165

Delay evaluation methodology of regular 16-bit Sqrt CSLA: The structure of the 16-bit Regular Square Root Carry Select Adder (Sqrt CSLA) has five groups of different size RCA. Only group 2 delay evaluation is discussed:

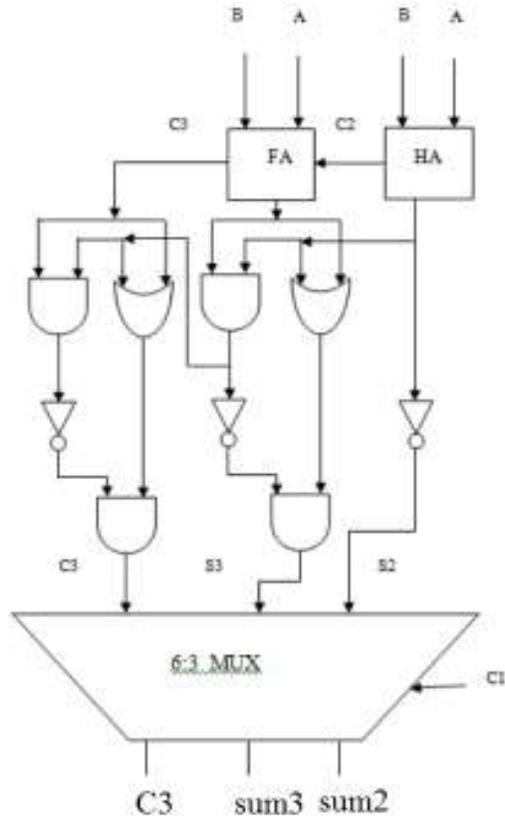
- The group 2 has two sets of 2-bit RCA. The regular CSLA (Mitra and Dutta, 2012) structure has two Ripple Carry Adder (RCA). One of RCA use with initial carry $C_{in} = 0$ and other with carry $C_{in} = 1$. The sum 3 ($t = 11$) is summation of S_3 and mux ($t = 3$) and sum 2 ($t = 10$) is summation of c_1 and mux, based on the delay values stated earlier (Mitra and Dutta, 2012) and thereby their respective arrival time.
- Except for group 2, the arrival time of mux selection input (Nair, 2013) is always greater than the arrival time of data outputs from the RCAs. Thus, the delay of group 3 to 5 is determined (Mitra and Dutta, 2012; Pandey *et al.*, 2013) respectively as follows:

$$\begin{aligned} \{c_6, \text{sum [6: 4]}\} &= c_3 [t = 10] + \text{mux} \\ \{c_{10}, \text{sum [10: 7]}\} &= c_6 [t = 13] + \text{mux} \\ \{c_{15}, \text{sum [15: 11]}\} &= c_{10} [t = 16] + \text{mux} \end{aligned}$$

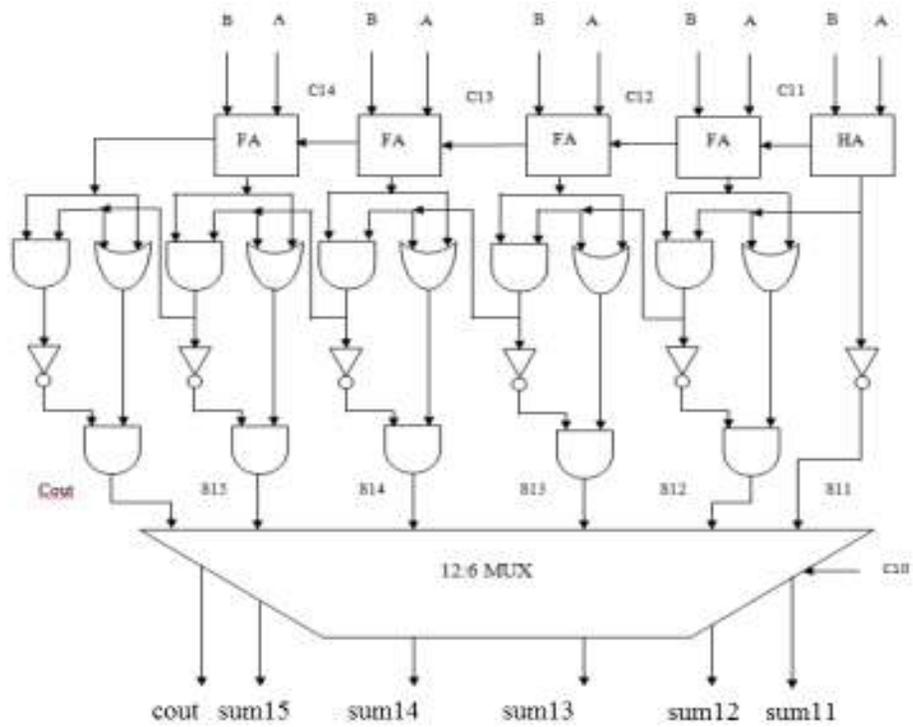
The one set of 2-bit RCA in group 2 has 2 FA for $C_{in} = 1$ and other set has 1 HA for $C_{in} = 0$. The area and total no. of gates can be calculated as follows:

$$\begin{aligned} \text{Gate Count} &= 57 \text{ (FA+HA+mux)} \\ \text{FA} &= 39 \text{ (3*13) (FA-Full Adder)} \\ \text{HA} &= 6 \text{ (1*6) (HA-Half Adder)} \\ \text{Mux} &= 12 \text{ (3*4)} \end{aligned}$$

Proposed Sqrt carry select adder: In this type of Adder, the block of Ripple Carry Adder with input carry as 1 has been replaced with a block of Binary to Excess-1 Converter (BEC) as shown in Fig. 2. This is done in order to reduce the area and power requirement of the previous conventional Carry Select Adder. The



(a)



(b)

Fig. 3: (a) Group 2 (modified CSLA), (b) group 5 (modified CSLA)

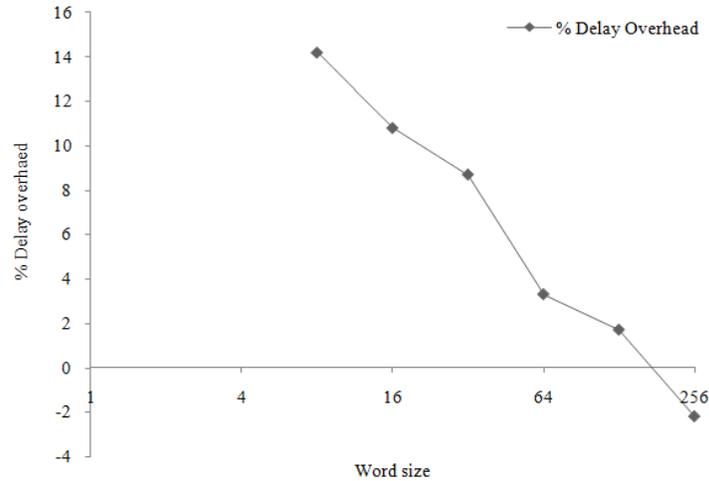


Fig. 4: Percentage of delay overhead

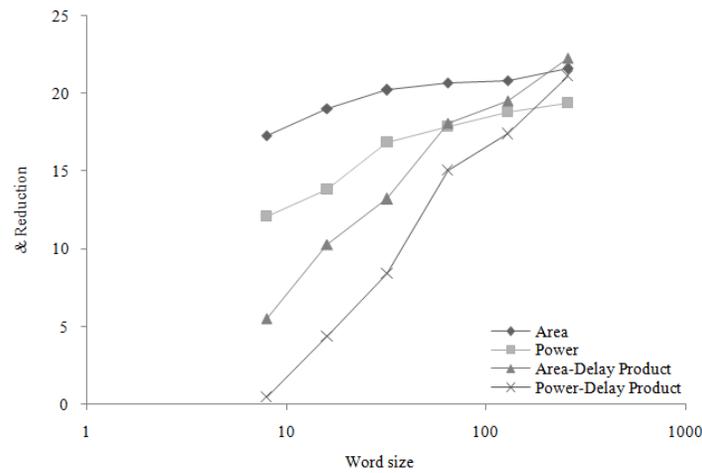


Fig. 5: Percentage reduction of product parameter

Table 2: Percentage reduction

Word size (bit)	Area	Area-delay	Power	Power-delay
8	17.30	5.50	12.10	0.46
16	19.02	10.30	13.81	4.34
32	20.20	13.20	16.87	8.41
64	20.69	18.10	17.84	15.05
128	20.80	19.50	18.78	17.40
256	21.58	22.28	19.40	21.10

Table 3: Implementation result

Word size	CSLA	Delay (nsec)	Area (um ²)	Power (μw)			Power-delay product (10 ⁻¹⁵)	Area-delay product (10 ⁻²¹)
				Leakage power	Switching power	Total power*		
8-bit	Regular	0.700	1134	0.043	96.021	96.065	67.2455	793.80
	Modified	0.800	0938	0.034	84.411	84.446	67.5568	750.40
16-bit	Regular	1.212	2472	0.095	226.311	226.407	274.4052	2996.06
	Modified	1.343	2002	0.070	195.305	195.370	260.5180	2688.56
32-bit	Regular	1.926	5246	0.199	504.093	504.293	971.2680	10103.79
	Modified	2.095	4188	0.152	424.497	424.649	889.6390	8773.86
64-bit	Regular	3.500	10694	0.407	997.391	997.798	3492.2930	37429.00
	Modified	3.616	8482	0.307	820.153	820.461	2966.7980	30670.91
128-bit	Regular	5.644	21961	0.826	2176.423	2177.249	12279.6300	123860.00
	Modified	5.736	17394	0.634	1837.932	1768.567	10144.5050	99771.98
256-bit	Regular	9.804	44684	1.672	4546.005	4547.678	44588.4350	438081.90
	Modified	9.598	35044	1.253	3665.546	3666.800	35193.9490	336352.30

*: Total power = Leakage power + Internal power + Switching power

maximum estimated areas of each group of the modified and regular SQR T CSLA are given in Table 1.

The area of each group is calculated manually by the no. of gates used in the structure. The percentage reduction of CSLA for different word sizes are given in Table 2.

Delay evaluation methodology of modified SQR T CSLA: Thirty two-bit modified SQR T CSLA structure is given in Fig. 2. The steps leading to the delay evaluation are given here Table 1 and 3.

The second group has a 2-bit RCA. Instead of another 2-bit RCA with $C_{in} = 1$, a 3-bit BEC is used which adds 1 to the output from 2-bit RCA. Based on the values of the Arrival time of selection input $c1$ of 6:3 mux is earlier than the $s3$ and $c3$ and later than the $s2$. Thus, the sum 3 and final $c3$ (output from mux) depend on $s3$ and mux and partial $c3$ (input to mux) and mux, respectively. An area count of CSLA is given in Table 1. Modified partial CSLA structure of group 2 and group 5 are given in Fig. 3a and b.

For the remaining groups the arrival time of mux selection input is always greater than the arrival time of data inputs from the BECs. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay. Comparing the delay values of the earlier models and the proposed model, the reduction in area, power and delay values are given in Table 2. The implementation results in terms of leakage, switching and total power are given in Table 3. These results are obtained by Cadence RTL compiler.

RESULTS AND DISCUSSION

The design proposed in this study has been developed using Verilog-HDL and synthesized in Cadence RTL compiler using typical libraries of TMS C 180 nm technology. Designs of CSLA were developed using structural Verilog module and synthesized using Xilinx ISE simulator, version 10.1 and the implementation is done in cadence RTL compiler.

The percentage reduction in the total power dissipation and the delay, with respect to the worst path of the flow is given in Table 2. The analysis shows that

there has been a considerable decrease in the power and delay with slight increase in the area compared to the earlier work (Ramkumar and Kittur, 2012).

The implementation results are as shown in Table 3. The percentage of delay overhead is as shown in Fig. 4.

The percentage reduction in the cell area, total power, power-delay product and the area-delay product as function of the bit size are shown in Fig. 5.

CONCLUSION

After comparing the different parameters of various adders with the proposed modified SQR T CSLA, it is evident that the power dissipation has been reduced to the desired extent with a slight increase in area. The proposed model provides a good tradeoff between the time and power consumption. Hence the modified 256-bit CSLA is more efficient for the VLSI hardware implementation. Further work is to be done in reducing the area and for higher order adders (512-bit), thus improving the overall system performance as such.

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