Research Journal of Applied Sciences, Engineering and Technology 8(11): 1289-1293, 2014
DOI:10.19026/rjaset.8.1098
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: January 06, 2014 Accepted: February 10, 2014 Published: September 20, 2014

Research Article

Critical Analysis Aspect of GaN HEMT Parasitic Elements and Its Effects on Power Performance of a SMPA

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Abstract: The study was conducted on the analysis of how the nonlinear behavior of the transistor affecting the drain efficiency could be minimized by integrating it in the output matching network of the power amplifier. In wireless communication, higher switching ability power amplifiers are a good choice for future advanced transmitters design. Minimizing all parasitic components is particularly very critical during the design of high-efficiency Switch-Mode Power Amplifiers (SMPA). To use the transistor in switching mode more efficiently, we analyzed some of the dominant parasitic components for better power performance of the transistor. Based on the proposed transistor model, a SMPA based on simplified class F architecture at 5.8 GHz using a Gallium Nitride High Electron Mobility Transistor (GaN HEMT) with the maximum output power of 47 dBm and high performance values of the PAE of 53.9% at peak with the power gain of 12 dB was designed. Load pull technique is used to find out the best load impedance of the amplifier.

Keywords: Class F, drain efficiency, load-pull, on-resistance, parasitic, switching mode, transistor parasitic

INTRODUCTION

The growing demand of reliable high data rates transmission in advanced communication systems, such as Wireless Communication, TV transmissions, Radar, requires an outstanding linearity condition. Some portable electronics such as cell-phones or base-stations are in an increasing pursuit of the efficiency to satisfy the requirement of long standby time and low cost. In order to ensure multimedia applications in small size, the Radio Frequency Integrated Circuit (RFIC) and digital signal processing modules are usually integrated into portable electronics. These requirements depend on the Power Amplifier (PA) in these devices. For the reliable transmission, the PA output power must be sufficient.

High efficiency improves thermal management, battery lifetime and has a direct impact on the operational costs. The high gain is not only required to reduce the number of amplifier stages required to deliver the expected output power, but also reduce the manufacturing cost as well as the size of the device. Beside these requirements, to achieve bandwidth demand good linearity is necessary. However the trade-off between the linearity and the output power efficiency requirements raise up. To develop GaN-based power switching devices, the advanced achievement related to the material quality improvement and process techniques in GaN microwave power devices (Kuroda *et al*., 2010; Gang *et al*., 2012; Zhang *et al*., 2003) should now be exploited and put in use during the power electronics design.

For better performances of communication systems, a high-speed switching ability of the transistor is most important parameter considered in this study. To satisfy above conditions, the parasitic components of the transistor were modeled and have to be minimized.

Rest of the study is organized as follows. The second part discusses the modeling and analysis of the transistor; the linear and non linear behaviors are introduced. The dynamic behavior was discussed at the end of this part. The third part the results and discussions are presented. Finally, the last part concludes this paper and indicates the summary of the work.

METHODOLOGY

Modeling and behavior analysis:

Ideal behavior of the transistor: In Switching-Mode Power Amplifiers (SMPA) designs, the transistor operates like a switch, as shown in Fig. 1. At the operating frequency, these types of PAs the transistor with quick switching capability manifests two kind of states, the ON-state and the OFF-state characterized by a low impedance and a high impedance respectively.

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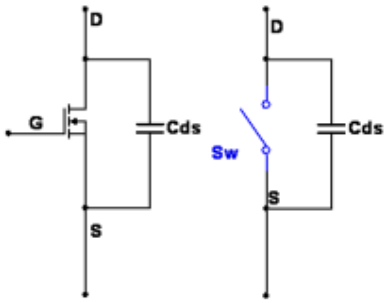
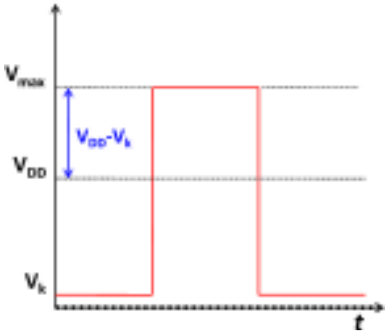
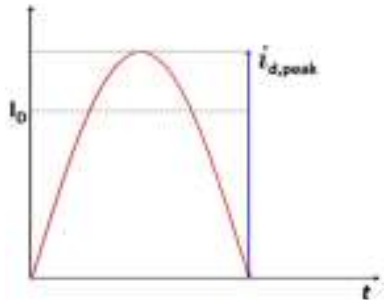


Fig. 1: The simplified model of the switching device



(a)



(b)

Fig. 2: The drain voltage and current waveforms of ideal class-F PA, (a) voltage waveform, (b) current waveform

These states are also used to describe the period of time when the device starts conducting and the period of time when the device stops conducting. This switching ability leads to accurate designs of SMPA like the class-F PA.

For Class F amplifier operation, the transistor acts like a switch. Drain current conducting phase parameter is θ = 90°, the drain voltage phase parameter is θ = 0°, this time voltage takes the form of a square wave and current wave is characterized by a half sine wave. For this class of amplifier, in ideal case there should not be any overlaying region between the voltage wave and the current wave on the switching-mode transistor.

To satisfy this condition, the voltage across the transistor must be zero just before the transistor turns to ON-state starts conducting the current. On the other side, the current through the transistor must return to zero just before the transistor turns to OFF-state (Grebennikov *et al*., 2012) as shown in the Fig. 2. Because there is no simultaneous superposition of the voltage and current, therefore the dissipated energy during the transition from one state to another state can be reduced to zero.

The Fourier series expansion of the voltage and current waveforms presented in the Fig. 2 are given, respectively in Eq. (1) and (2):

$$V(\theta) = V_{DD} - \frac{4(V_{DC} - V_k)}{\pi} \sum_{n=1,3,5,\ldots} \frac{\sin n\theta}{n} \tag{1}$$

$$I(\theta) = i_{d,peak}\left(\frac{1}{\pi} + \frac{1}{2}\sin(\theta) - \frac{2}{\pi} \sum_{n=2,4,6,\ldots} \frac{\cos n\theta}{n^2 - 1}\right) \tag{2}$$

From Eq. (1) and (2) we can deduce the DC voltage and DC voltage current as:

$$V_0 = V_{DD} \tag{3}$$

$$I_0 = \frac{i_{d,peak}}{\pi} \tag{4}$$

The voltage and the current at the fundamental frequency are:

$$V_{fund} = \frac{4(V_{DD} - V_k)}{\pi}\sin(\theta) \tag{5}$$

$$I_{fund} = \frac{i_{d,peak}}{2}\sin(\theta) \tag{6}$$

From Eq. (3) to (6) we can compute the Load resistance Eq. (7) and the drain efficiency Eq. (8) to be:

$$R_{Load} = \frac{V_{fund}}{I_{fund}} = \frac{8}{\pi}\frac{(V_{DD} - V_k)}{i_{d,peak}} \tag{7}$$

$$\eta_d = \frac{(V_{DD} - V_k)}{V_{DD}}\sin^2(\theta) \tag{8}$$

Considering $V_k = R_{on} \cdot i_{d,peak}$, the expression of the drain efficiency becomes:

$$\eta_d = \frac{(V_{DD} - R_{on} \cdot i_{d,peak})}{V_{DD}}\sin^2(\theta) \tag{9}$$

Assuming V_{DD} to be a constant value, we find that the efficiency is a function of the Ron, drain peak current and operating phase. For a given square wave voltage and a half sine wave current the phase equals to 90°. Considering the transistor as working as perfect

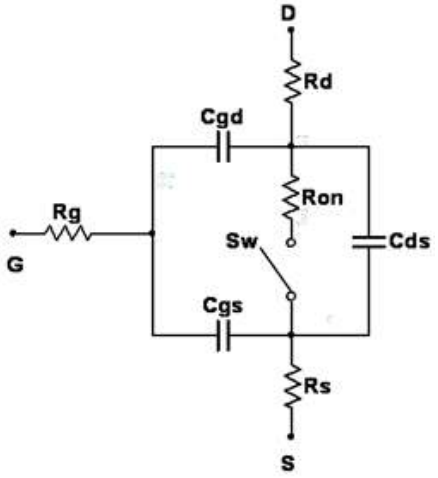


Fig. 3: The proposed switching-mode transistor model

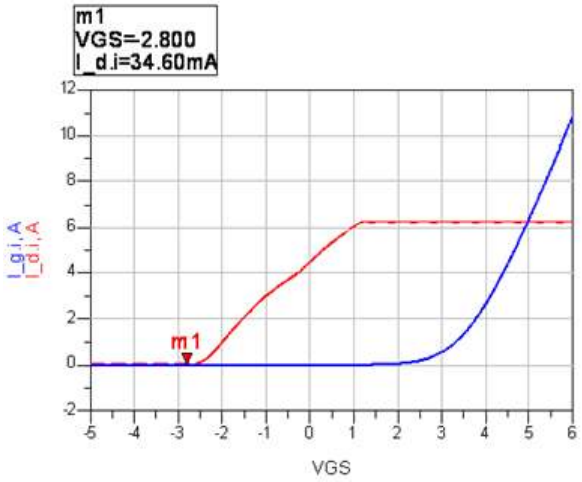


Fig. 4: Ig-Vgs, Id-Vgs characteristics for GaN HEMT (V_{DD} = 28V)

switch V_k should be equal to zero and the 100% of drain efficiency is achieved, but this is not the case in the real world. From this assumption, the Ron and θ are the main parameters which affect the power dissipation through the transistor; they should be analyzed and minimized to improve the drain efficiency.

Nonlinear behavior of the transistor: The transistor has different kind of parasitic elements which affect its performance in its switching operation and then make it not working like a real switch. Parasitic elements like capacitances and the ohmic loss through the drain to source path of the device are the most dominant parasitic. The simplified basic switch-based model of high frequency transistor is presented in the Fig. 3 as an equivalent circuit. The intrinsic parasitic are deeply analyzed as the most important parasitic, the extrinsic elements are also discussed. The proposed model comprises the drain-source (output) capacitance Cds, the gate-drain (feedback) capacitance Cgd (Wren and Brazil, 2005) and the gate-source (input) capacitance Cgs. The access Resistances at the drain (Rd), source (Rs) and gate (Rg) are also incorporated.

Nonlinear output resistance of the device: For a specific value of threshold voltage V_{ON}, if the input drive levels Vin exceeding V_{ON} the switch has an ON-Resistance (R_{on}) and for Vin small than V_{ON} the switch has an OFF-resistance (R_{off}) as we can find it in the equation Eq. (10) and (11):

$$R_{out} = \begin{cases} R_{on} & for \quad V_{in} > V_{on} \\ R_{off} & for \quad V_{in} < V_{on} \end{cases} \tag{10}$$

$$R_{on} = \frac{3}{4}\frac{V_{DS}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DS}\right) \tag{11}$$

where, λ is the channel-length modulation.

Ron is time-varying, nonlinear and dependent on the operation point of the transistor. For fixed operating point in class F PA design as shown in the Fig. 4, in static analysis the bias point is chosen as the static Power (P_{DC}) dissipated through the transistor could be minimized. The Id dependency upon Vgs is even more pronounced. Ron is virtually independent of the supply voltage. As I_{DSAT} is proportional to the size of the device then Ron depends on the device structure for a given technology.

In dynamic analysis, for operating frequency f, in the cut-off region the output impedance of the device is affected by Cds. When the switch is in the ON-state, Cds is shunted by Ron smaller (the low-resistive channel), the output impedance is mainly determined by the value of R_{ON}. Whereas, if the transistor is fully OFF, R_{0ff} is larger than the reactance Xc = 1/ωCds, in this condition, the output impedance is mainly influenced by the value of Cds, hence, dominates the device's electrical behavior. Thus, measuring the value of Cds at fixed value of supply-voltage (Negra *et al*., 2007; Park *et al*., 2012; Rabaey *et al*., 2003) is sufficient to attain an accurate precision in SMPA design.

Dynamic behavior of GaN devices: The nonlinear gate-to-drain capacitance Cgd is the most important and the most varying capacitance (Aflaki *et al*., 2009), as it is located between the input and the output terminal of the device, the value of Cgd affects both input and output impedance and provides a negative feedback from the power circuit to the gate drive circuit, which stands as one reason for the mutual couple of oscillation between gate drive stage and power stage (Li *et al*.,

2011). Modeling its behavior precisely is therefore necessary to obtain good precision. The nonlinear capacitance model is defined by the nonlinear expression in Eq. (12) (Rabaey *et al*., 2003):

$$C_{gd} = \frac{C_{gdo}}{\left(1 - V_{gd}/\phi_0\right)^m} + \frac{\tau_T I_S}{\phi_T} e^{V_{gd}/n\phi_T} \quad (12)$$

where, Cgd0, ϕ_0, m, ϕ_T, Is and n represent the small-signal capacitance, junction potential, grading coefficient, transit time, saturation current and emission coefficient respectively. For Is≈0, Cgd depends on Cgd0, ϕ_0 and m.

RESULTS AND DISCUSSION

Another limitation to the performance of the transistor in PA design is its intrinsic delay. The simplified circuit given in the Fig. 5 is used to extract the total drain capacitance, at the fixed operating bias point; we find that the value of Cds is a function of drain-to-source voltage V_{DS}.

The intrinsic delay of this transistor can be computed using the expression Eq. (13). Considering the access transistors Rd and Rs, we can easily verify that such an increase in resistance Rd and Rs does not significantly affect the minimum drain delay (intrinsic delay):

$$\tau_{ds} = kR_{on}C_{ds} \quad (13)$$

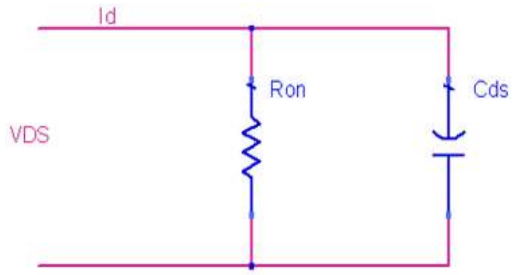


Fig. 5: Total drain capacitance extraction

At higher frequencies, device capacitances and package capacitance and inductance can be significant; these all parasitic elements affect the power performance of the SMPA. To speed up the F class PA design and taking the device power enhancement in consideration the load-pull and source-pull techniques were used.

In our design, the Load pull technique is used to find out the best load impedance of the amplifier. As shows in the Fig. 6 we find that to achieve the desired output power of 47 dBm, we need the load impedance of 20.877-j25.384 and in this case we obtain a PAE greater than 60%.

The output network design beyond 500 MHz is difficult to realize with discrete components because the wavelength becomes comparable with the physical network element dimensions, resulting in various losses severely degrading the PA performance. Thus, in this design the distribution element realizations and the simulation result of the designed matched output network is given in the Fig. 7.

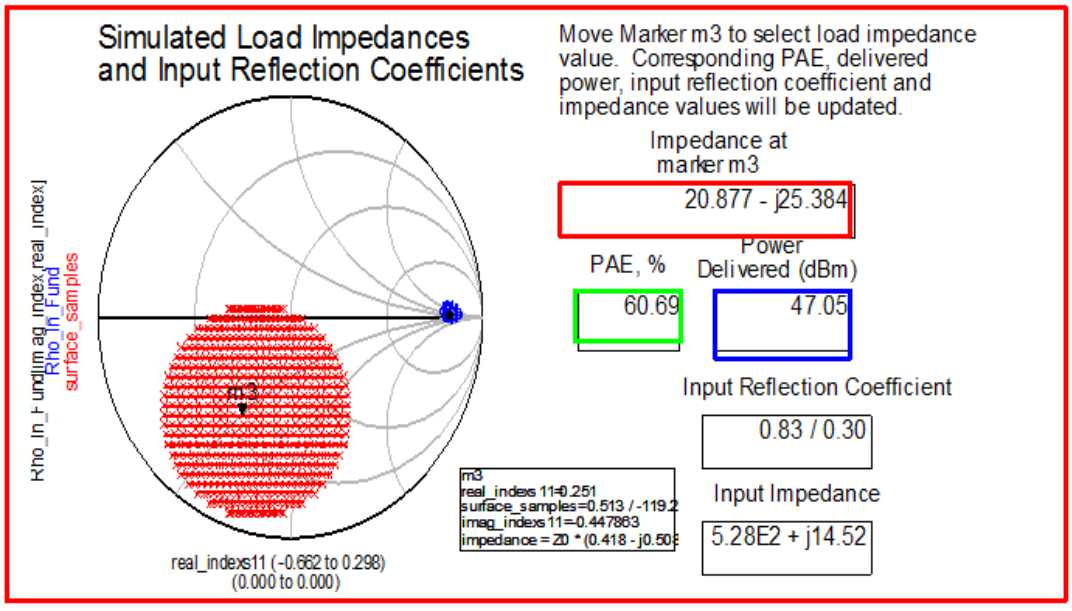


Fig. 6: The load-pull simulation result for the desired output power

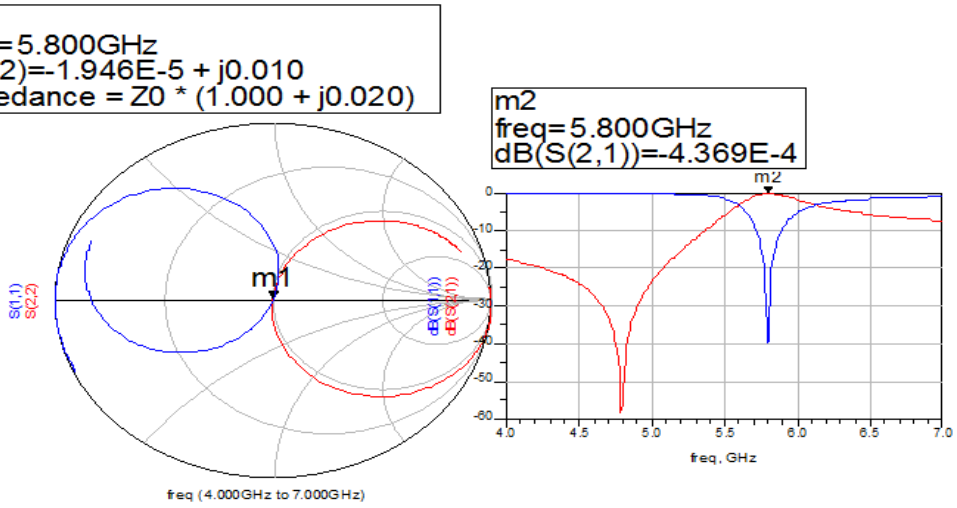


Fig. 7: The matched output network

CONCLUSION

To decrease the output power losses of the power amplifier design, a deep analysis on the switching ability of the transistor was conducted; the model of main parasitic element affecting the transistor performance in SMPA design is provided and analyzed. In this study we presented the impact of the nonlinear behavior of the transistor to the drain efficiency reduction which affects the PAE of the SMAP. Beside these, we presented the significant role the supply voltage plays to the improvement of the switching delay of the device. During the PA design, selecting the right transistor is one of the most critical points; the parameter discussed in this study are to be noticed and will help the high frequency power amplifier design engineers to overcome this stage. A PA based on simplified class F architecture operating at 5.8 GHz using a GaN HEMT transistor with the maximum output power of 47 dBm. To minimize the parasitic effect on the circuit performance, the design optimization was performed and the high performance optimized values of the PAE greater than 54% at peak with the power gain of 12 dB was obtained.

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