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Research Article

A Novel Space Vector Technique for the Direct Three-level Matrix Converter

C. Agees Kumar, T.S. Sivarani and S. Joseph Jawhar
Department of EEE, Arunachala College of Engineering for Women, Vellichanthai, India

Abstract: This study proposes a novel Direct Torque Control (DTC) method for the Direct Three level Matrix Converter (DTMC), which uses both the input phase voltage vectors (short vectors) and the input line voltage vectors (long vectors). The problem of voltage imbalance at the input filter capacitance due to the use of the short vectors is addressed with an additional voltage hysteresis comparator. With the errors of torque, flux, sin Ψ and the neutral point voltage, an Optimum Switching Table (OST) is designed for the DTMC. The OST generates the necessary switching signals for the DTC of the DTMC. The DTMC topology with the modified ISVM technique reduces the THD at the output. The proposed DTMC Indirect Space Vector pulse width Modulation (ISVM) technique uses the idea of multilevel inverter SVM technique along with the proposed neutral current balancing strategy for generating the firing pulses. The switching loss model for the DTMC is developed and the performance of the DTMC is compared with that of the Conventional Matrix Converter (CMC). The performance of the proposed DTC technique for the DTMC is evaluated through simulation to explain the reduced torque ripple characteristics. To validate the proposed DTMC ISVM technique, a 3 kVA direct multilevel matrix converter prototype was developed.

Keywords: Conventional matrix converter, direct three level matrix converter, direct torque control, indirect space vector pulse width modulation

INTRODUCTION

The Matrix Converter is an attractive topology of power converter for variable speed AC drive applications, which converts the AC to AC in a single stage. The advantages of the matrix converter are its capability of producing a variable output voltage with unrestricted input and output frequency, the absence of electrolytic capacitors and the potential to increase the power density, reduced size, reduced weight and better input power quality. However, industrial applications of these converters are limited because of some practical issues such as complex control strategies, high susceptibility to input power disturbances, common mode voltage effects and low voltage transfer ratio. Recently, matrix converters have experienced a resurgence of attention due to the advancements in the semiconductor device industry and the growth of processor technologies, which promises practical implementation of matrix converters in the control of drives. The matrix converter is the force-commutated version of the cyclo-converters (Huber and Borojevic, 1989), which overcomes the disadvantage of the conventional cyclo-converter such as the limitations in the frequency conversion, rich output voltage harmonics and increased number of switches (Rashid, 2005; Fa-Hai *et al*., 1994). The indirect or the sparse matrix converter is a cascade of the controlled rectifier and inverter topologies without a DC link in between (Boost and Ziogas, 1988).

The voltage stresses on the power devices can be reduced by using Multi-Level Inverters (MLIs) (Celanovic and Boroyevich, 2000; Lopez *et al*., 2008; Aneesh *et al*., 2009). MLIs permit the use of lower rating power supplies and power devices for achieving higher output power rating. Using the same idea in the matrix converters, a new family of converters called multilevel matrix converters evolved with different concepts:

i) Replacing each bidirectional switch in the CMC with n cells, each cell consisting of a capacitor connected to the centre of the H Bridge (Erickson and Al-Naseem, 2001; Erickson *et al*., 2006). This topology generates multi-level output but at the cost of a more complicated circuit configuration and modulation strategy.
ii) Modifying the topology of the IMC with additional switches, which makes available two different voltages levels at the output, i.e., the phase and the line voltages (Meng *et al*., 2010). This topology is effective for two-level and three-level voltage conversion with less complicated circuit configuration and modulation strategy as compared

Corresponding Author: C. Agees Kumar, Department of EEE, Arunachala College of Engineering for Women, Vellichanthai, India

to (i). Modified IMC based three-level converter uses the diode clamped multi-level space vector technique (Meng *et al*., 2010) on the inverter side and the conventional space vector technique on the rectifier side. The main objective of this study is to develop a new class of Direct Three-level Matrix Converter (DTMC) along with its modulation techniques and to analyze its performance with the existing techniques.

MATERIALS AND METHODS

Problem formulation: The objective of this study is to develop a new DTMC topology namely, the direct three-level matrix converter, which requires three bidirectional switches of lower ratings (phase voltage rated) and the CMC topology. The structure is a 4×3 matrix converter that facilitates the increase in the output voltage levels by making the source neutral available to the load terminals. In addition to the multilevel operation, the converter also has the ability to control bi-directional power flow. The proposed DTMC is evaluated by simulation and hardware experimentation. The modulation strategy of the DTMC uses the multi-level space vector modulation technique along with the proposed neutral current balancing strategy. The same is implemented using the Xilinx based system generator facility, which is available as a toolbox in MATLAB R2010a, along with an FPGA.

Methodology: A DTMC in its very generic form, shown in Fig. 1, consists of three arms that are connected to the source and one arm connected to the star point (neutral) of the input filter capacitances. Figure 1 depicts the general configuration of the proposed DTMC structure which consists of a CMC and a neutral point connecter.

Indirect matrix converter representation for the DTMC: The proposed DTMC topology consists of an array of 4×3 bi-directional switches, which includes the 3×3 switches of the CMC and three additional switches for making the neutral point of the input filter capacitance to be available at the load terminals. Equation (1) and (2) give the output voltages and the input currents of the DTMC:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} & S_{Na} \\ S_{Ab} & S_{Bb} & S_{Cb} & S_{Nb} \\ S_{Ac} & S_{Bc} & S_{Cc} & S_{Nc} \end{bmatrix} \times \begin{bmatrix} V_A \\ V_B \\ V_C \\ 0 \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} I_A \\ I_B \\ I_C \\ I_N \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \\ S_{Na} & S_{Nb} & S_{Nc} \end{bmatrix} \times \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad (2)$$

Since the DTMC is supplied by a voltage source, the input phases must never be shorted and due to the inductive nature of the load, the output phases must never be left open. These constraints are realized by Eq. (3):

$$S_{Aj} + S_{Bj} + S_{Cj} + S_{Nj} = 1 \; j \in \{a, b, c\} \quad (3)$$

The DTMC can be decoupled into an Indirect Three-level Matrix Converter (ITMC) consisting of a Fictitious Two-level Converter (FTC-input converter)

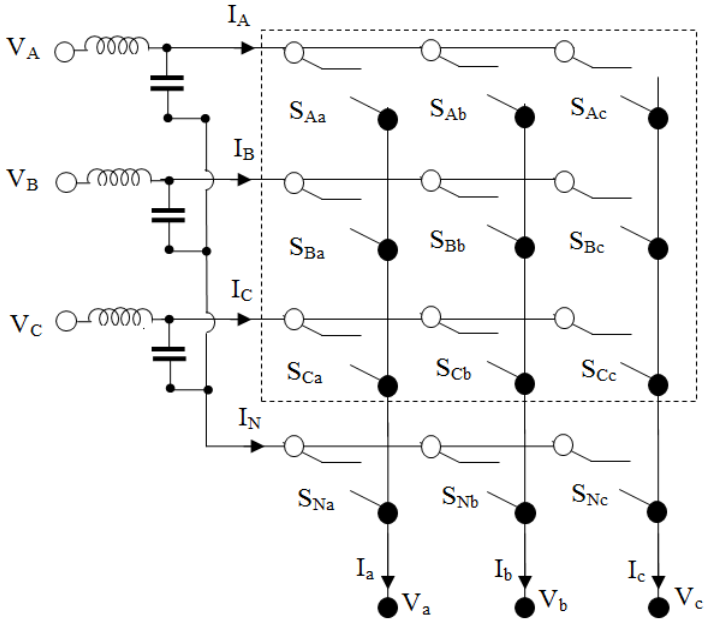


Fig. 1: Topology of the direct three-level matrix converter

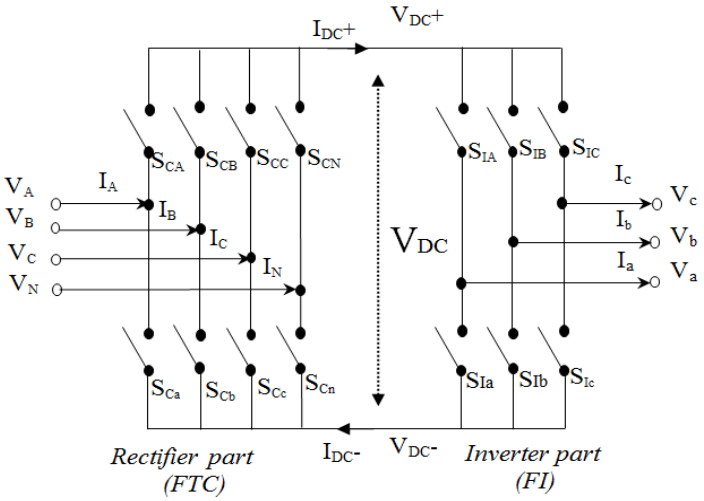


Fig. 2: Topology of the indirect three-level matrix converter

Table 1: Space vectors for the fictitious two-level converter

Type	Vector	$\begin{bmatrix}S_{CA} & S_{CB} & S_{CC} & S_{CN}\\ S_{Ca} & S_{Cb} & S_{Cc} & S_{Cn}\end{bmatrix}$	I_A	I_B	I_C	$I_N = I_0$	I_{in}	$\angle \mathbf{I_{in}}$	$\mathbf{V_{DC}}$
Active long vectors	I_{L1}[AB]	$\begin{bmatrix}1000\\0100\end{bmatrix}$	$+I_{DC}$	$-I_{DC}$	0	0	$\sqrt{3}I_{DC}$	330^0	V_{AB}
	I_{L2}[AC]	$\begin{bmatrix}1000\\0010\end{bmatrix}$	$+I_{DC}$	0	$-I_{DC}$	0	$\sqrt{3}I_{DC}$	30^0	V_{AC}
	I_{L3}[BC]	$\begin{bmatrix}0010\\0001\end{bmatrix}$	0	$+I_{DC}$	$-I_{DC}$	0	$\sqrt{3}I_{DC}$	90^0	V_{BC}
	I_{L4}[BA]	$\begin{bmatrix}0100\\1000\end{bmatrix}$	$-I_{DC}$	$+I_{DC}$	0	0	$\sqrt{3}I_{DC}$	150^0	V_{BA}
	I_{L5}[CA]	$\begin{bmatrix}0010\\1000\end{bmatrix}$	$-I_{DC}$	0	$+I_{DC}$	0	$\sqrt{3}I_{DC}$	210^0	V_{CA}
	I_{L6}[CB]	$\begin{bmatrix}0010\\0100\end{bmatrix}$	0	$-I_{DC}$	$+I_{DC}$	0	$\sqrt{3}I_{DC}$	270^0	V_{CB}
Active short vectors	I_{P1}[AN]	$\begin{bmatrix}1000\\0001\end{bmatrix}$	$+I_{DC}$	0	0	$-I_{DC}$	I_{DC}	0^0	V_{AN}
	I_{P2}[NC]	$\begin{bmatrix}0001\\0010\end{bmatrix}$	0	0	$-I_{DC}$	$+I_{DC}$	I_{DC}	60^0	V_{NC}
	I_{P3}[BN]	$\begin{bmatrix}0100\\0001\end{bmatrix}$	0	$+I_{DC}$	0	$-I_{DC}$	I_{DC}	120^0	V_{BN}
	I_{P4}[NA]	$\begin{bmatrix}0001\\1000\end{bmatrix}$	$-I_{DC}$	0	0	$+I_{DC}$	I_{DC}	180^0	V_{NA}
	I_{P5}[CN]	$\begin{bmatrix}0010\\0001\end{bmatrix}$	0	0	$+I_{DC}$	$-I_{DC}$	I_{DC}	240^0	V_{CN}
	I_{P6}[NB]	$\begin{bmatrix}0001\\0100\end{bmatrix}$	0	$-I_{DC}$	0	$+I_{DC}$	I_{DC}	300^0	V_{NB}
Zero vectors	I_Z	$\begin{bmatrix}1&0&0&0\\1&0&0&0\end{bmatrix}\begin{bmatrix}0&1&0&0\\0&1&0&0\end{bmatrix}\begin{bmatrix}0&0&1&0\\0&0&1&0\end{bmatrix}\begin{bmatrix}0&0&0&1\\0&0&0&1\end{bmatrix}$					0		0

$I_{in}=\sqrt{I_\alpha{}^2+I_\beta{}^2}$; $\angle I_{in}= \tan^{-1}\frac{I_\beta}{I_\alpha}$

and a Fictitious Inverter (FI-output converter), as shown in Fig. 2.

The FTC consists of three phase arms and one neutral arm. Switching ON any of the two phase arms leads to the line voltage being available at the FDCB and switching ON any one phase arm with the neutral arm leads to the phase voltage being available at the FDCB. This results in twelve active voltage vectors on the rectifier side. This decoupled representation simplifies the control of the input current and the output voltage in DTMC, as described in the next section.

Space vector modulation technique for the DTMC: The switching function for the DTMC is represented as the product of the rectifier switching function and the inverter switching function and is given by Eq. (4):

$$\begin{bmatrix}S_{Aa} & S_{Ba} & S_{Ca} & S_{Na}\\ S_{Ab} & S_{Bb} & S_{Cb} & S_{Nb}\\ S_{Ac} & S_{Bc} & S_{Cc} & S_{Nc}\end{bmatrix} = \begin{bmatrix}S_{IA} & S_{Ia}\\ S_{IB} & S_{Ib}\\ S_{IC} & S_{Ic}\end{bmatrix} \times \begin{bmatrix}S_{CA} & S_{CB} & S_{CC} & S_{CN}\\ S_{Ca} & S_{Cb} & S_{Cc} & S_{Cn}\end{bmatrix} \quad (4)$$

The switching states for synthesizing the required currents and voltages are described in the following subsections.

The fictitious two-level converter stage: Assuming that the output of the FTC is a constant current source

I_{DC}, the space vector for all valid switching states are determined by Eq. (5) to (7):

$$I_\alpha = I_A + I_B \cos\frac{2\pi}{3} + I_C \cos\frac{4\pi}{3} \quad (5)$$

$$I_\beta = I_B \sin\frac{2\pi}{3} + I_C \sin\frac{4\pi}{3} \quad (6)$$

$$I_0 = I_A + I_B + I_C \quad (7)$$

As described earlier, switching ON the neutral arm causes the current to flow in the source neutral resulting in the space vector having a component along the I_0 axis. Table 1 gives the space vector components for different valid switching states and Fig. 3a shows the space vectors distribution:

Vectors represented by I_{Li} (active long vectors) are conventional rectifier space vectors, which do not contribute to the neutral current. Vectors represented by I_{Pi} (active short vectors) contribute to the neutral current. To ensure that the input current is sinusoidal, the reference space vector must lie on the αβ plane requiring the neutral current to be zero on application of the vector I_{Pi}. This is carried out by applying equally the adjacent I_{Pi} vectors, which lie on the upper and the lower halves of the αβ plane. This ensures that the average neutral current is zero over a switching period. The example in Table 2 explains the same.

This solution to the neutral current balancing problem (Celanovic and Boroyevich, 2000) introduces virtual vectors I_{VPi}, which lie completely on the αβ plane, as given in Table 3 and shown in Fig. 3b.

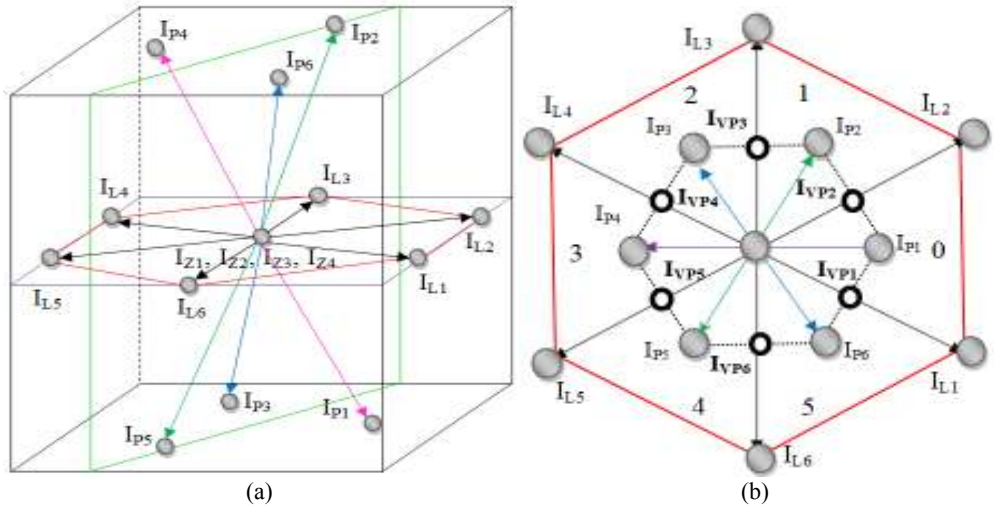


Fig. 3: (a) Space vectors of the FTC (b) space vectors and virtual vectors of the FTC

Table 2: Neutral current balancing and virtual vector synthesis

Switching time	Applied vectors	I_A	I_B	I_C	I_N	V_{DC}
$\frac{T_s}{2}$	I_{P6}	0	$-I_{DC}$	0	$+I_{DC}$	V_{NB}
$\frac{T_s}{2}$	I_{P1}	$+I_{DC}$	0	0	$-I_{DC}$	V_{AN}
T_s	$I_{VP1}=\frac{1}{2}I_{P6}+\frac{1}{2}I_{P1}$	$+\frac{1}{2}I_{DC}$	$-\frac{1}{2}I_{DC}$	0	0	$\frac{1}{2}V_{AB}$

Table 3: Virtual current space vectors

Virtual vectors	Sharing vectors	I_A	I_B	I_C	$I_N = I_0$	I_{in}	$\angle I_{in}$	V_{DC}
I_{VP1}[AN]	I_{P6},I_{P1}	$+\frac{1}{2}I_{DC}$	$-\frac{1}{2}I_{DC}$	0	0	$\frac{\sqrt{3}}{2}I_{DC}$	330^0	$\frac{1}{2}V_{AB}$
I_{VP2}[NC]	I_{P1},I_{P2}	$+\frac{1}{2}I_{DC}$	0	$-\frac{1}{2}I_{DC}$	0	$\frac{\sqrt{3}}{2}I_{DC}$	30^0	$\frac{1}{2}V_{AC}$
I_{VP3}[BN]	I_{P2},I_{P3}	0	$+\frac{1}{2}I_{DC}$	$-\frac{1}{2}I_{DC}$	0	$\frac{\sqrt{3}}{2}I_{DC}$	90^0	$\frac{1}{2}V_{BC}$
I_{VP4}[NA]	I_{P3},I_{P4}	$-\frac{1}{2}I_{DC}$	$+\frac{1}{2}I_{DC}$	0	0	$\frac{\sqrt{3}}{2}I_{DC}$	150^0	$\frac{1}{2}V_{BA}$
I_{VP5}[CN]	I_{P4},I_{P5}	$-\frac{1}{2}I_{DC}$	0	$+\frac{1}{2}I_{DC}$	0	$\frac{\sqrt{3}}{2}I_{DC}$	210^0	$\frac{1}{2}V_{CA}$
I_{VP6}[NB]	I_{P5},I_{P6}	0	$-\frac{1}{2}I_{DC}$	$+\frac{1}{2}I_{DC}$	0	$\frac{\sqrt{3}}{2}I_{DC}$	270^0	$\frac{1}{2}V_{CB}$

Figure 4a shows the sector zero of the space vector diagram of the FTC. Each sector consists of two active long vectors, two active virtual short vectors and four zero vectors. To synthesize the required reference input current and the FDCB voltage, the three nearest current vectors (Busquets-Monge *et al*., 2004) are selected, as shown in Fig. 4b, depending on the modulation index m_c of the FTC.

In order to identify the region in which the reference vector lies, equations of the three lines are derived and shown in Fig. 5. Table 4 gives the rules for identifying the region in which the reference vector lies in the FTC for different values of modulation indices m_c.

Duty cycles of the selected vectors for different regions are computed using Eq. (8), where (x_i, y_i) are the coordinates of the selected vector I_i and d_i is its duty cycle. X and Y are the coordinates of the reference vector I_{REF} and are given by Eq. (9):

$$\begin{bmatrix} x_1 & x_2 & x_3 \\ y_1 & y_2 & y_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} X \\ Y \\ 1 \end{bmatrix} \tag{8}$$

$$X = m_c \times \cos\theta_c \;\; \& \;\; Y = m_c \times \sin\theta_c \tag{9}$$

While computing the duty cycle, the sector in Fig. 6a is rotated as shown in Fig. 6b. The coordinates are chosen according to the region in which the reference vector lies, as shown in Fig. 6b. Table 5 gives the duty cycles derived for different regions.

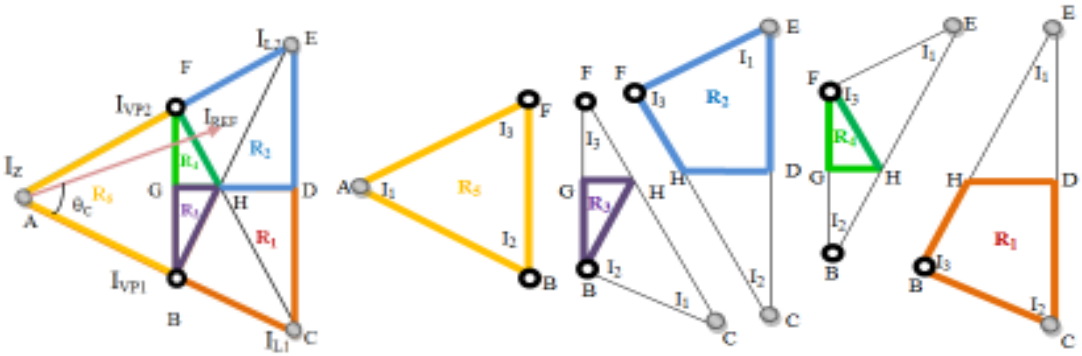


Fig. 4: (a) Sector region identification of the FTC (b) region vector identification of the FTC

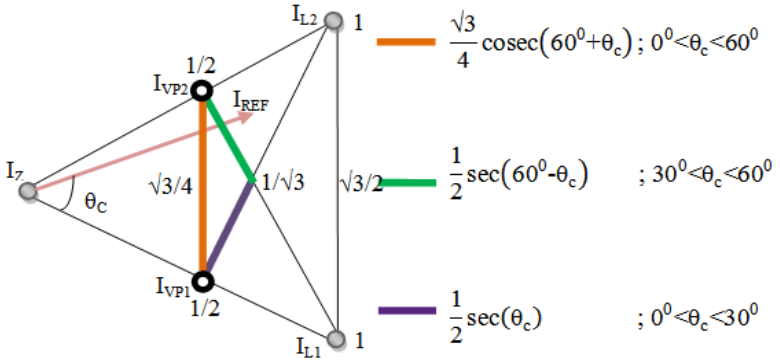


Fig. 5: Equations of lines used for identifying regions in the FTC

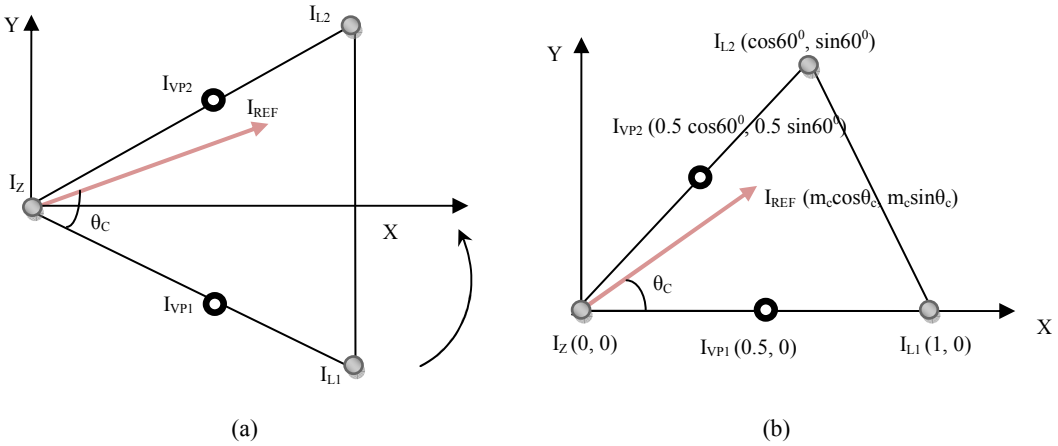
Table 4: Region identification for a given I_{REF}

Region	Conditions
R_1	$m_c > \frac{1}{2}\sec(\theta_c)\,;\ 0^0<\theta_c<30^0$
R_2	$m_c > \frac{1}{2}\sec(60^0-\theta_c)\,;\ 30^0<\theta_c<60^0$
R_3	$\frac{\sqrt{3}}{4}\mathrm{cosec}(60^0+\theta_c) < m_c \leq \frac{1}{2}\sec(\theta_c)\,;\ 0^0<\theta_c<30^0$
R_4	$\frac{\sqrt{3}}{4}\mathrm{cosec}(60^0+\theta_c) < m_c \leq \frac{1}{2}\sec(60^0-\theta_c)\,;\ 30^0<\theta_c<60^0$
R_5	$m_c \leq \frac{\sqrt{3}}{4}\mathrm{cosec}(60^0+\theta_c)\,;\ 0^0<\theta_c<60^0$

Table 5: Duty cycles for different regions in a given sector

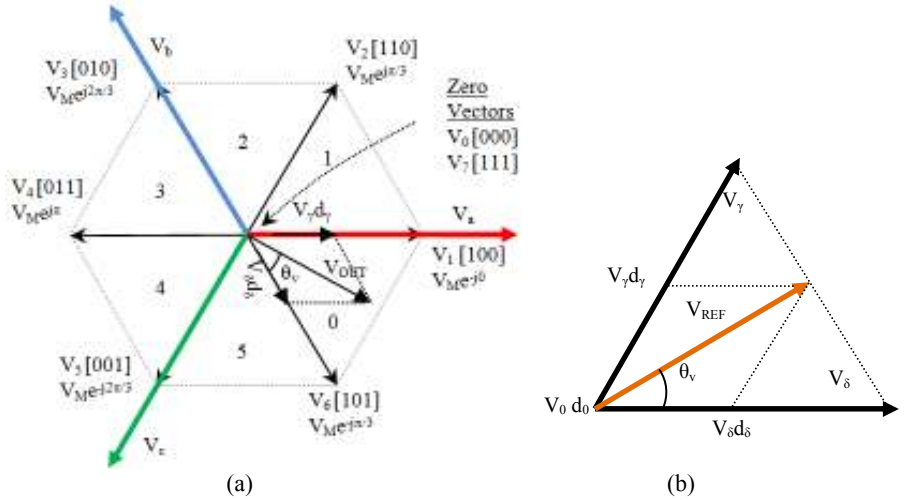
	Duty cycle		
Region	d_1- I_1	d_2- I_2	d_3 - I_3
R_1	$\frac{2}{\sqrt{3}} m_c \sin(\theta_c)$	$2\, m_c \cos(\theta_c) - 1$	$2 - \frac{4}{\sqrt{3}} m_c \sin(60^0+\theta_c)$
R_2	$2\, m_c \sin(30^0+\theta_c) - 1$	$\frac{2}{\sqrt{3}} m_c \sin(60^0-\theta_c)$	$2 - \frac{4}{\sqrt{3}} m_c \sin(60^0+\theta_c)$
R_3	$\frac{4}{\sqrt{3}} m_c \sin(60^0+\theta_c) - 1$	$\frac{4}{\sqrt{3}} m_c \sin(60^0-\theta_c)$	$2 - 4\, m_c \cos(\theta_c)$
R_4	$\frac{4}{\sqrt{3}} m_c \sin(60^0+\theta_c) - 1$	$2 - 4\, m_c \sin(30^0+\theta_c)$	$\frac{4}{\sqrt{3}} m_c \sin\theta_c$
R_5	$1 - \frac{4}{\sqrt{3}} m_c \sin(60^0+\theta_c)$	$\frac{4}{\sqrt{3}} m_c \sin(60^0-\theta_c)$	$\frac{4}{\sqrt{3}} m_c \sin\theta_c$

θ_c: The angle of I_{REF} within the sector; m_c: The inverter zero compensated converter modulation index discussed later and is given in Eq. (14)



(a) (b)

Fig. 6: (a) Sector 1 and (b) sector 1 rotated



(a) (b)

Fig. 7: (a) Space vectors of the FI and (b) sector and duty cycle allocation

The fictitious inverter stage: The conventional SVPWM is implemented in the inverter stage. This consists of six active voltage vectors and two zero voltage vectors, as shown in Fig. 7. To generate the required reference vector V_{OUT}, adjacent active vectors V_γ, V_δ and a zero vector V_0 are selected whose duty cycles d_γ, d_δ and d_0 are given by Eq. (10):

$$d_\gamma = \sin(60^0 - \theta_v),\ d_\delta = \sin(\theta_v) \text{ and } d_0 = 1 - (d_\gamma + d_\delta) \quad (10)$$

where, θ_v is the angle of V_{OUT} within a sector. The output voltage of the inverter can be adjusted by any one of the two schemes:

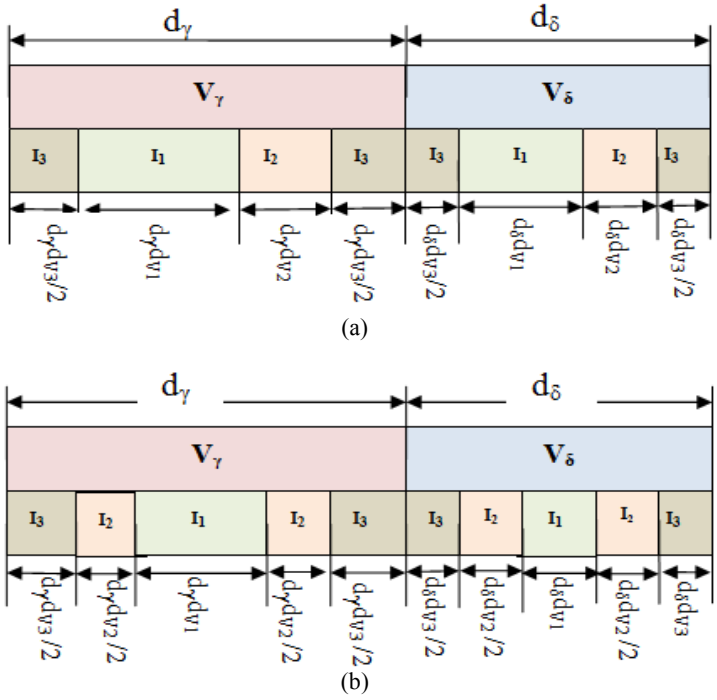


Fig. 8: (a) Switching pattern of the DTMC for the regions R_1 and R_2 (b) switching pattern of the DTMC for the regions R_3, R_4 and R_5

- Changing the FDCB voltage to the inverter
- Changing the modulation index m_v of the inverter

The second scheme is not used for reasons explained in the next paragraph and hence $m_v = 1$. The FDCB voltage can be varied by changing the modulation index m_c' of FTC as given in Eq. (11):

$$m_c' = \frac{\sqrt{3}}{2} m_{DTMC} \quad (11)$$

where, m_{DTMC} is the required modulation index of the DTMC. At higher modulation indices, the FTC reference vector, I_{in}, lies in any one of the regions R_1, R_2, R_3 or R_4. These regions do not use any zero vectors for the modulation. Simultaneous use of the zero vectors at the inverter stage would cause the output voltage to become zero. This is not consistent with the idea of multilevel switching techniques as it increases the THD at the output. To decrease the THD of the DTMC, zero vectors are not used at the inverter stage, which does not allow for the change in modulation index m_v. With the elimination of the zero vectors, the duty cycles for active vectors are recomputed as given in Eq. (12). This increases the output voltage vector as given by Eq. (13). Thus the reference vector is brought outside the inscribed circle of the space vector hexagon leading to an over modulation condition:

$$d_\gamma' = \frac{d_\gamma}{d_\gamma + d_\delta} \;\&\; d_\delta' = \frac{d_\delta}{d_\gamma + d_\delta} \quad (12)$$

$$V_{OUT}' = d_\gamma' V_\gamma + d_\delta' V_\delta = \frac{V_{OUT}}{d_\gamma + d_\delta} \quad (13)$$

The increase in the output voltage vector is compensated by adjusting the FDCB voltage by modifying the modulation index of the FTC dynamically, as given by Eq. (14):

$$m_c = \frac{\sqrt{3}}{2} m_{DTMC}(d_\gamma + d_\delta) \quad (14)$$

Figure 8 shows the allocation of the switching vectors in a sampling period for a particular inverter sector and for different regions of the converter sector. The period of the virtual vector is divided into two, during which the adjacent upper and lower active short vectors of the corresponding virtual vector is applied. The real-time switching pattern for the DTMC is computed for each vector combination of the FTC and the FI using Eq. (4). Figure 8a shows the switching pattern for the DTMC for regions R_1 and R_2 when only one active virtual vector is used. Figure 8b shows the switching pattern for the DTMC for regions R_3, R_4 and R_5 when two active virtual vectors are used.

DTMC operation under abnormal input conditions: From Eq. (14) it can be shown that within a sector, m_c reaches the peak once when $(d_\gamma + d_\delta) = 1$ and reaches the minimum value twice when $(d_\gamma = 0)$ or $(d_\delta = 0)$ and this repeats for all the six sectors. Hence the dynamic variation of the m_c introduces a sixth harmonic

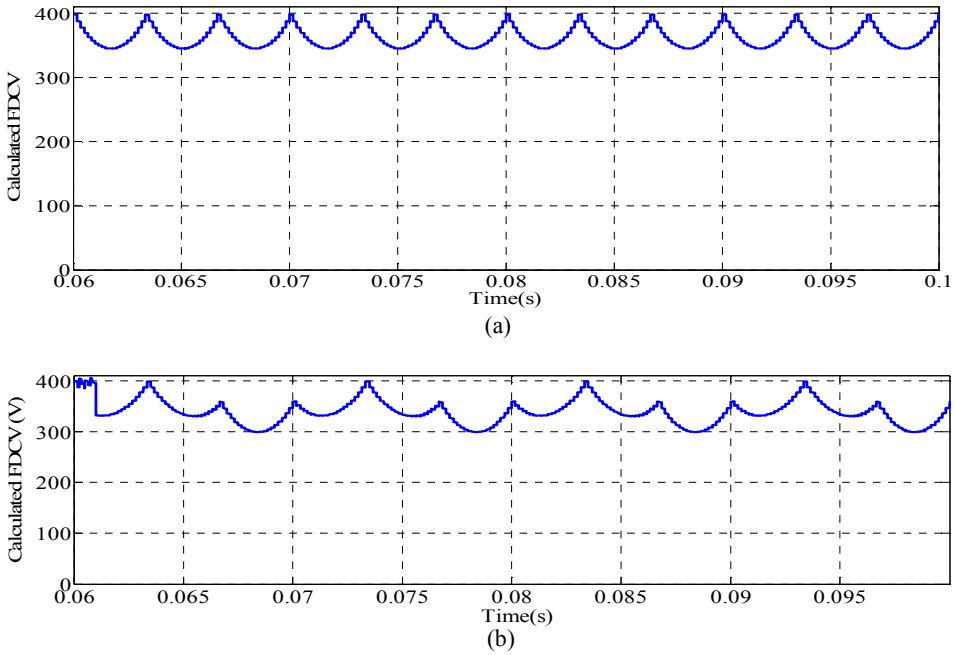


Fig. 9: (a) Calculated FDCV with a balanced input voltage (b) calculated FDCB voltage with an unbalanced input voltage

component $6f_i$ at the FDCB, as shown in Fig. 9a, where f_i is the fundamental frequency of the input voltage.

It was shown in chapter 4 that an input unbalance introduces a second harmonic component $2f_i$ at the FDCB of the CMC. Hence, the FDCB voltage of DTMC, as shown in Fig. 9b, contains two components $6f_i$ and $2f_i$ during the input unbalance.

The instantaneous variation can be determined by Eq. (15), where V_R, V_S and V_T are the FDCB voltage on applying the switching vectors I_1, I_2 and I_3, respectively:

$$V_{DC} = d_1 \times |V_R| + d_2 \times |V_S| + d_3 \times |V_T| \quad (15)$$

To mitigate the effects of the unbalance at the output, as explained in chapter 4, the input voltage of the FI must be limited to the minimum of the FDCB voltage V_{DC} over an input cycle expressed as V_{DC_Min}. This is achieved by dynamically modifying m_c, as given in Eq. (16). This mitigates the effect of unbalance and harmonics in the output currents while the input current harmonics are left uncompensated:

$$m_c = \frac{\sqrt{3}}{2} m_{DTMC} \left(d_\gamma + d_\delta\right) \times V_{DC\_Min}/V_{DCF} \quad (16)$$

MODELING OF LOSSES IN THE CMC AND THE DTMC

There are three types of losses in power semiconductor devices namely the ON, the OFF and the switching losses. The power loss in the device when it is "OFF" is negligible compared to its power loss when it is either "ON" or when it is undergoing transition. The power loss in the device during its 'ON' state is called the conduction loss while the power losses in the device during its transition ('ON' to 'OFF' or vice-versa) states is called the switching loss. Conduction loss is the product of the voltage drop across the device and the current through the device, when it is in the 'ON' state. Switching loss is proportional to the product of blocking voltage and conduction current at the instant of switching; and if this is significant, it is termed as hard switching loss (Bierhoff and Fuchs, 2004). If the switching occurs when either the current through the device or the voltage across the device is nearly zero, the commutation is referred to as 'soft switching' and the switching loss in the device is negligible. For an IGBT, there are two types of losses during hard switching: T_{on_losses} and T_{off_losses}, associated with the device turn-ON and turn-OFF process, respectively. For a diode, the switching loss is caused by reverse recovery mechanism that occurs only during the diode turn-OFF. Hence, the turn-ON loss for a diode is not considered.

Conduction loss modeling for the CMC and the DTMC: From Eq. (3), it can be seen that in each phase only one switch conducts at any given time. Hence, there is always only one IGBT that conducts and only one diode that conducts at an output phase of the CMC and the DTMC. Equation (17) and (18) give the conduction loss and the conduction energy of one output phase in each switching cycle:

$$C_{Losses}(v_d, i_L) = v_{d_{IGBT}}(i_L) \times i_L + v_{d_{DIODE}}(i_L) \times i_L \quad (17)$$

$$E_c(v_d, i_L) = \int_0^{Ts} C_{Losses}(v_d, i_L)\, dt \quad (18)$$

where,

$v_{d_{IGBT}}(i_L)$: The ON state voltage drop in the IGBT
$v_{d_{DIODE}}(i_L)$: The ON state voltage drop in the diode and given by Eq. (19) and (20):

$$v_{d_{IGBT}}(i_L) = x + y \times i_L^{\ z} \quad (19)$$

$$v_{d_{DIODE}}(i_L) = m + n \times i_L^{\ k} \quad (20)$$

where, x, y, z, m, n and k are constants that are obtained from the curve fitting equation of V_{ce}-I_c characteristics given in the datasheet of the device used. Then the average conduction loss over an interval T, for the CMC and the DTMC, is give by Eq. (21):

$$C_{L\_Avg} = \frac{1}{T}\int_0^T C_{Losses}(t)\, dt \quad (21)$$

Switching loss modeling for the CMC and the DTMC: During switching transients, the switching energy is described by Eq. (22) (Wang and Venkataramanan, 2006; Apap *et al*., 2003):

$$E_{sw}(v_{Block}, i_L) = E_{swR} \times (v_{Block} \times i_L) / (V_R \times i_R) \quad (22)$$

where, V_R, i_R and E_{swR} are, respectively the voltage, current and switching energy of the device at the rated V_R and i_R. From the four step commutation procedure, it can be seen that when commutation happens between the bidirectional switch S_1 to switch S_2 under the condition of $V_{in}>0$ and $I_{out}>0$, commutation losses do not occur for switches S_1^-, S_2^+ and S_2^-. This is because the switches S_1^- and S_2^- do not block any voltage and the switch S_2^+ does not conduct current. This creates only a turn OFF loss for the switch S_1^+. Similarly, S_2 to S_1 transition creates a turn ON loss for the switch S_1^+ and a turn OFF loss for the diode D_2^-. Table 6 summarizes the switching energy losses for commutation between S_1 and S_2 evaluated for all conditions of input voltages and output currents.

From Table 6, it can be generalized that two commutation events, i.e.:

- First phase to second phase transition and
- Second phase to first phase transition within a switching cycle produces three switching losses namely

Table 6: Switching energy losses for switch S_1 to switch S_2 transition

	I_{out} +		I_{out} -	
Switch transition	$S_1 \rightarrow S_2$	$S_2 \rightarrow S_1$	$S_1 \rightarrow S_2$	$S_2 \rightarrow S_1$
V_{in} +	E_{off}	$E_{on} + E_{rr\_D}$	$E_{on} + E_{rr\_D}$	E_{off}
V_{in} -	$E_{on} + E_{rr\_D}$	E_{off}	E_{off}	$E_{on} + E_{rr\_D}$

- An IGBT ON loss
- An IGBT OFF loss
- A Diode OFF loss

Hence $E_{swR} = E_{on} + E_{off} + E_{rr\_D}$ where, E_{on} and E_{off} are the switching energy for the IGBT ON and IGBT OFF switchings at the rated V_R and i_R. E_{rr_D} is the DIODE OFF switching energy at the rated V_R and i_R. In general, for a particular transition from the input phase x to the input phase y and vice-versa the switching loss is given by Eq. (23):

$$E_{sw}(v_{xy}, i_L) = (E_{on} + E_{iff} + E_{rr\_D}) * (|v_{xy}| * i_L) / (V_R * i_R) \quad (23)$$

From the T_{delay}-I_c characteristics of the datasheet, T_{on}, T_{off} and T_r are identified. Equation (24) gives the switching power loss:

$$S_{Losses}(v_{xy}, i_L) = \left(\frac{E_{on}}{T_{on}} + \frac{E_{off}}{T_{off}} + \frac{E_{rr\_D}}{T_r}\right) * (|v_{xy}| * i_L) / (V_R * i_R) \quad (24)$$

Switching energy calculation for the CMC: Switching losses depend on the modulation technique. In this study, a double-sided space vector switching technique is selected for the CMC as well as the DTMC. It can be seen that the optimized switching technique (Nielsen *et al*., 1996) leads to eight commutation events over all the three output phases in a switching cycle T_s. Four of these commutation events occur in an output phase and two commutation events each occur in the other two output phases.

From Fig. 10, it can be seen that the total switching energy of the CMC over a sampling time T_s is given by Eq. (25):

$$E_{sw} = K \,.\, (|v_{AC}|.\, i_a + |v_{BC}|.\, i_b + (|v_{AB}| + |v_{AC}|).\, i_c) \quad (25)$$

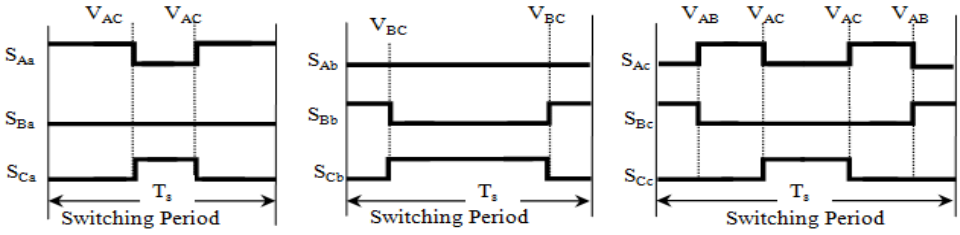


Fig. 10: Commutation events of the CMC in a switching period for voltage sector 1 and current sector 1

Table 7: Commutation events in a switching cycle T_s

	Converter sector -Y and inverter sector -X (regions of converter sector)				
Commutation events	R_1	R_2	R_3	R_4	R_5
Line voltage commutation	6	6	4/2	2/4	0
Phase voltage commutation	14	14	22	22	20

where, $K = (E_{on} + E_{off} + E_{rr\_D}) / (V_R \times i_R)$. For other voltage and current sectors, Eq. (25) can be generalized as Eq. (26):

$$E_{sw} = K (x\, i_a + y\, i_b + z\, i_c) \quad (26)$$

where, x, y and z take any of the values $|v_{AB}|$, $|v_{BC}|$, $|v_{AC}|$, $(|v_{AB}| + |v_{BC}|)$ or $(|v_{AB}| + |v_{AC}|)$ depending on the sectors of the current and the voltage.

Switching energy calculation for the DTMC: In the DTMC, two types of commutation events occur namely:

- The line commutation where the blocking voltage is the line voltage
- The phase commutation where the blocking voltage is the phase voltage

Extending the optimized indirect space vector switching's for the DTMC, the number of commutation events for a particular voltage sector X and different regions of current sector Y is calculated and given in Table 7. Equation (27) to (31) give the total switching energy of the DTMC over a sampling time T for the voltage sector 1 and different regions of the current sector 1.

Region 1:

$$E_{sw\_R1} = K . (|v_{AN}|. i_a + (|v_{BC}| + |v_{CN}| + |v_{BN}|). i_b + vAB+vAC+ 2vAN+vBN+vCN.ic \quad (27)$$

Region 2:

$$E_{sw\_R2} = K . (|v_{AN}|. i_a + (|v_{BC}| + 2|v_{CN}|). i_b + vAB+vAC+ 2vAN+ 2vCN.ic \quad (28)$$

Region 3:

$$E_{sw\_R3} = K . (3|v_{AN}|. i_a + (|v_{BC}| + |v_{CN}| + |v_{BN}|). i_b + vAB+3vAN+ vBN+2vCN.ic \quad (29)$$

Region 4:

$$E_{sw\_R4} = K . (3|v_{AN}|. i_a + (|v_{CN}| + |v_{BN}|). i_b + vAC+3vAN+vBN+ 2vCN.ic \quad (30)$$

Region 5:

$$E_{sw\_R5} = K . (2|v_{AN}|. i_a + (|v_{BN}| + 2|v_{CN}|). i_b + vBN+2vAN+2vCN.ic \quad (31)$$

The switching and conduction losses for the DTMC were derived and compared with those for the CMC. A complete loss model was developed using the SIMULINK blockset in MATLAB. Through simulations, switching energy losses for different regions for different sectors of the current and the voltage are calculated using the above procedure and results obtained are discussed and presented in the next section.

RESULTS AND DISCUSSION

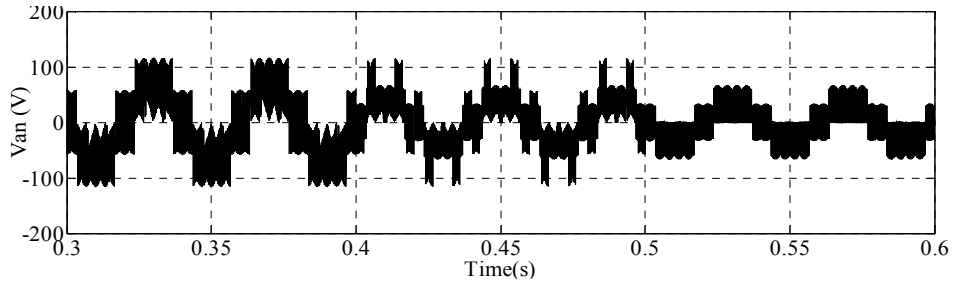
To evaluate the performance of the proposed topology with the modified space vector technique, simulation with R-L load was performed. Table 8 gives the simulation parameters.

For modulation indices between $\sqrt{3}/4$ and $\sqrt{3}/2$, the output voltage switches between the active long vectors and the active short vectors but for lower modulation indices, the output voltage switches between the active short vectors and the zero vectors. Figure 11 shows the output phase voltages, output line voltages, input currents and output currents for the voltage transfer ratio that is changed from 0.72 to 0.5 at 0.4 sec and 0.5 to 0.25 at 0.5 sec. The harmonic content of the input and the output currents increase with decrease in the voltage transfer ratio. In the CMC, the peak of the output voltage is $\sqrt{3}$ times the input voltage for all values of modulation indices. However, in the DTMC, the peak of the output voltage is $\sqrt{3}$ times the input voltage for the modulation indices greater than $\sqrt{3}/4$ while the peak of the output voltage is $\sqrt{3}/2$ times the input voltage for modulation indices lesser than $\sqrt{3}/4$. This leads to lower switching stress on the power devices in the case of the DTMC.

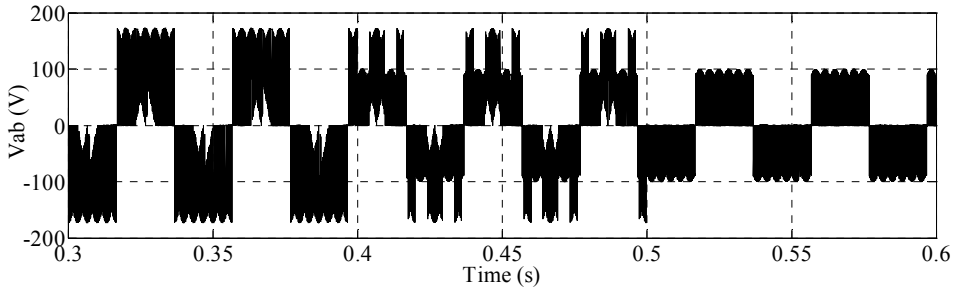
A 20% unbalance in the phase B was introduced. In addition, second and third harmonics with magnitudes of 4 and 7% of the fundamental respectively were added to all the three phases as shown in Fig. 12a. By dynamically modifying the modulation index, as explained in the previous section, the effect of the unbalance and harmonics has been mitigated in the output voltages and currents, as shown in Fig. 12b and d. The unbalanced input currents are shown in Fig. 12c.

Table 8: Simulation parameters for the DTMC topology

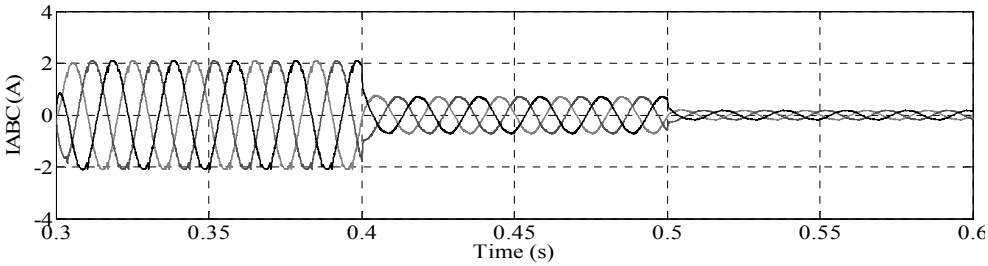
Quantity	Value
R-L load	R = 20 Ω, L = 21 mH
Input phase voltage	100 V
Input voltage frequency	50 Hz
Input filter	L = 2 mH, C = 35 μF
Output voltage frequency	25 Hz
Switching frequency	6 kHz
Modulation index	0.72, 0.5, 0.25



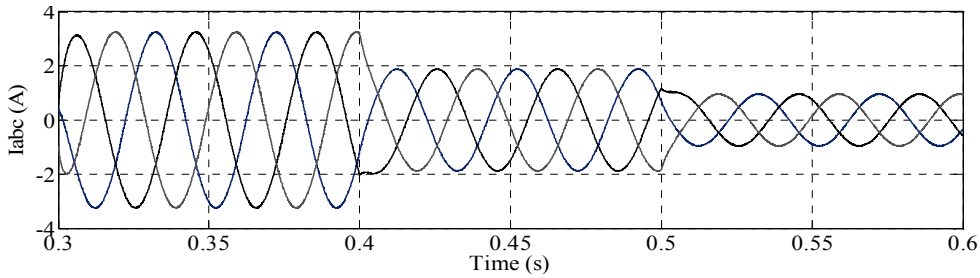
(a)



(b)

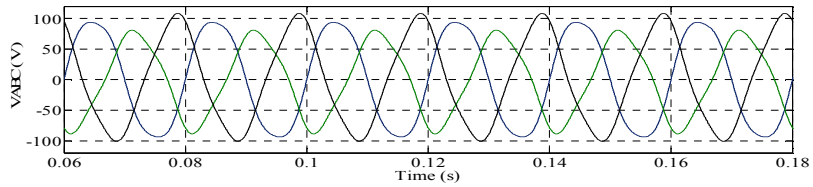


(c)

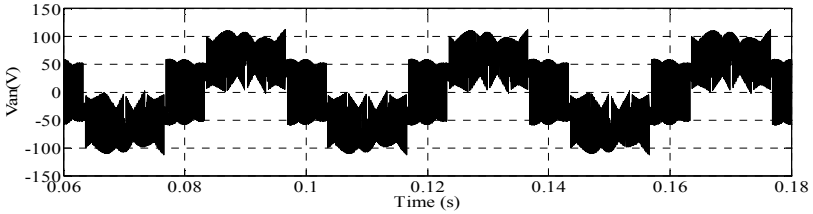


(d)

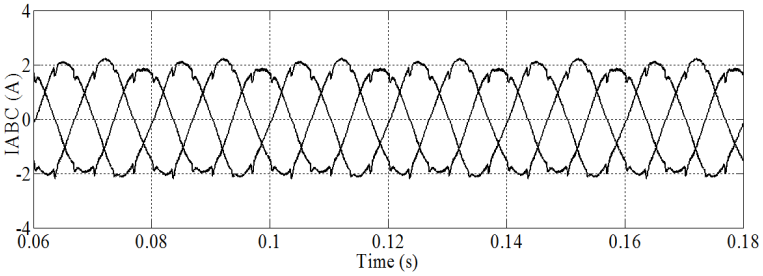
Fig. 11: Performance of the DTMC with a balanced supply for different modulation indices (0.72, 0.5, 0.25) (a) output phase voltage, (b) output line voltage, (c) input phase current, (d) output phase current



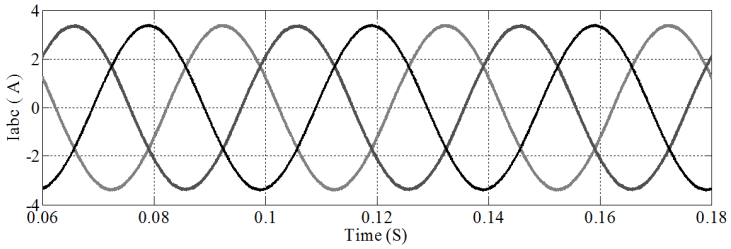
(a)



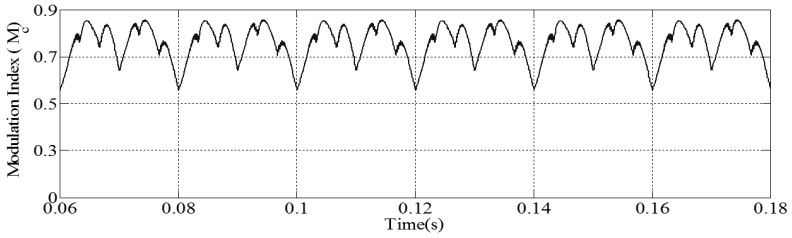
(b)



(c)



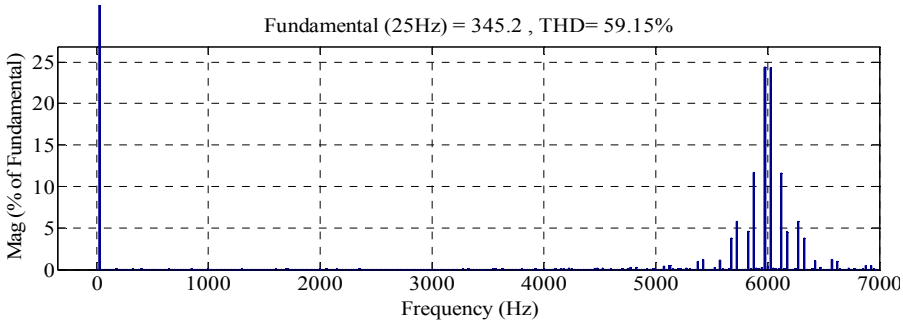
(d)



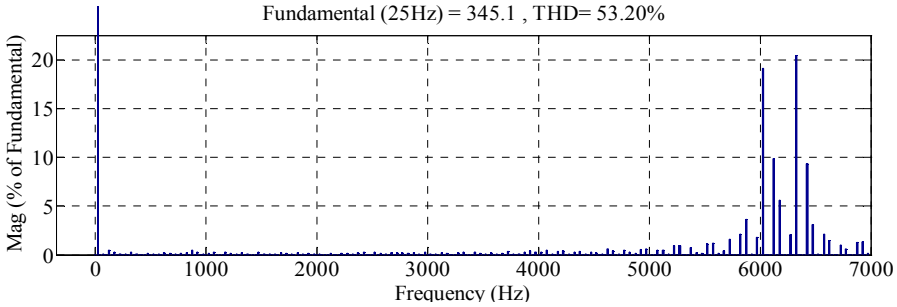
(e)

Fig.12: Performance of the DTMC with an unbalanced supply (a) output phase voltage, (b) output line voltage, (c) input phase current, (d) output phase current, (e) modulation index

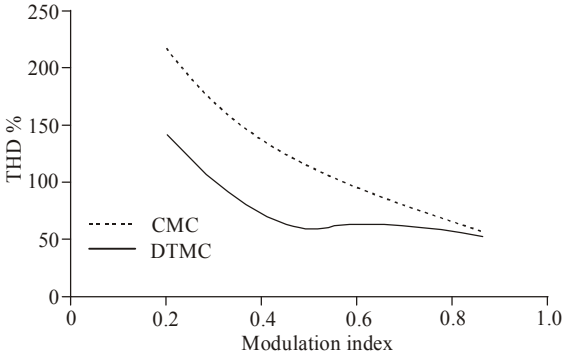
Figure 13 to 15 present a quantitative comparison between the CMC and the DTMC. Simulation was carried out for the CMC and the DTMC for a Modulation Index (MI) of 0.866 and the THD of the output voltage are shown in Fig. 13a and b. At the maximum modulation index of 0.866, the THD for the DTMC reduces by 10% when compared to the CMC. The THD content of the output voltage for the CMC and the DTMC, for all modulation indices, is presented in Fig. 13c. It can be seen that the DTMC has a better (lower) THD than the CMC for all modulation indices. In the DTMC, for modulation indices varying from 0.866 to 0.45, the current vector lies in any of the regions of R_1, R_2, R_3, or R_4 and the THD is almost constant as zero vectors are not selected. When the current vector is in the region R_5 (MI<0.4), the THD of



(a)

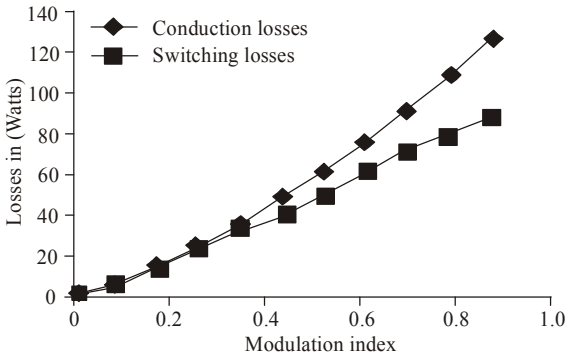


(b)

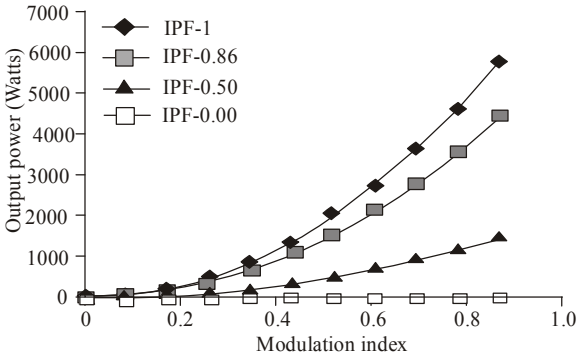


(c)

Fig. 13: Output voltage THD for MI of 0.866 (a) CMC, (b) DTMC, (c) output voltage THD for the CMC and the DTMC with 6 kHz switching frequency for different MI



(a)



(b)

Fig. 14: (a) Losses vs. MI and (b) output vs. MI (different IPF)

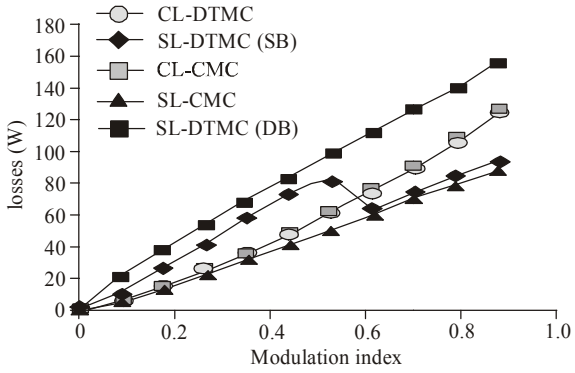


Fig. 15: Conduction and switching losses for the DTMC and the CMC for different values of MI

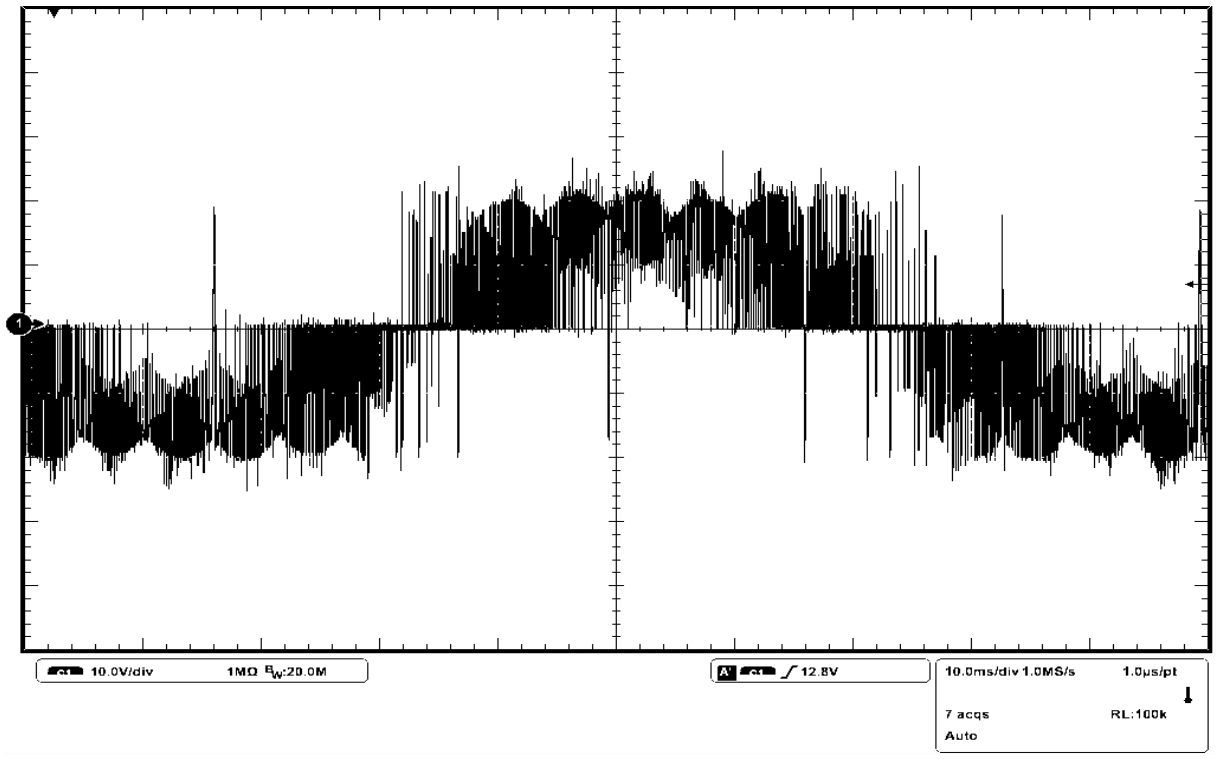
the DTMC rises linearly with modulation index, as in the case of the CMC, because of the use of the zero vectors.

At very low modulation index, the THD for the DTMC reduces by approximately 58% as compared to the CMC due to the use of phase vectors. From Fig. 14a, it can be observed that the conduction losses are always greater than the switching losses in the CMC, for different values of MIs. Figure 14b shows that as the input power factor decreases, the output power of the converter also decreases.

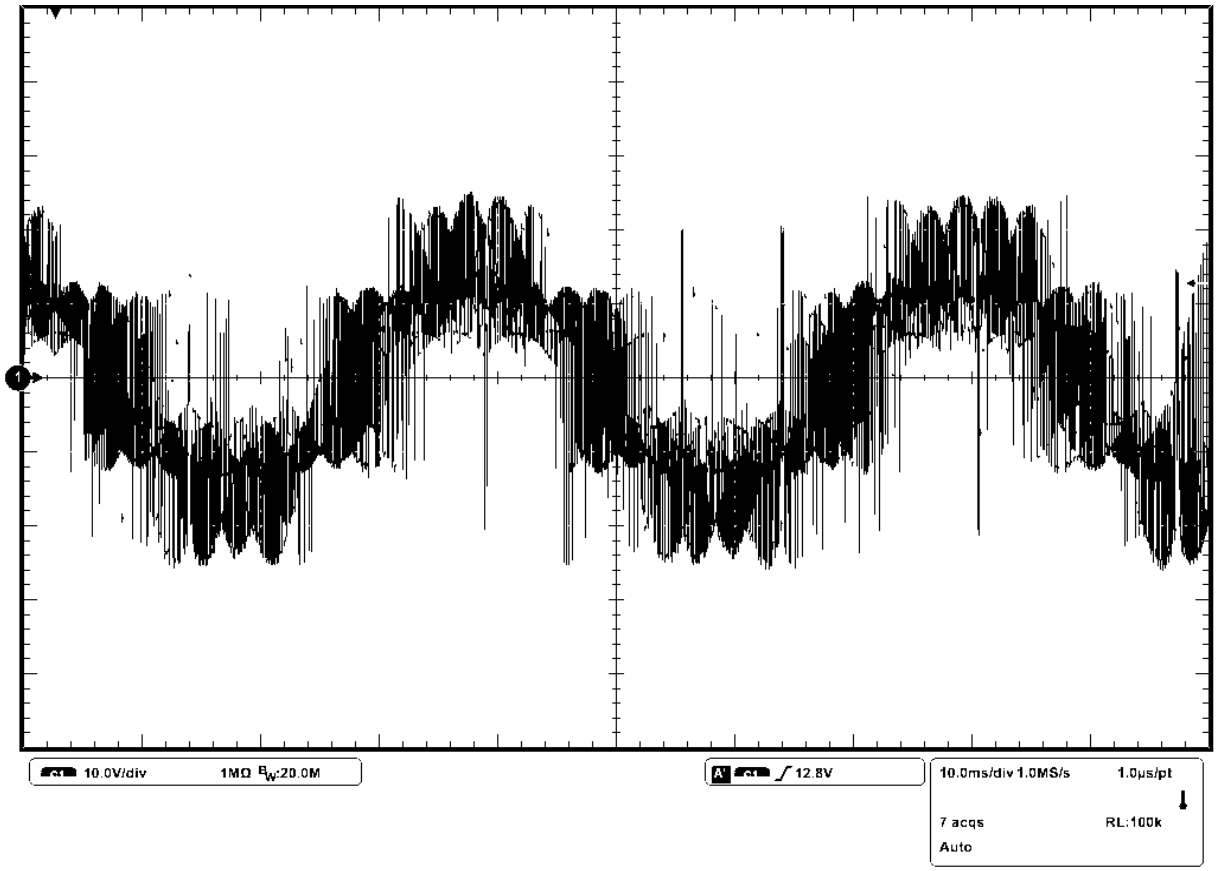
The conduction losses for the DTMC and the CMC are the same under all operating conditions. However, the switching losses for the DTMC are higher than the switching losses of the CMC for all MIs, since the switching events are more in the DTMC than in the CMC. With a double side banded SVM, the DTMC exhibits higher switching losses for all values of MIs. Nevertheless, for the single sided SWM, the DTMC exhibits higher switching losses for lower values of MIs and lower switching losses for higher values of MIs. This is because the switching events of the regions R_3, R_4 and R_5 are very high compared to the switching events of the regions R_1 and R_2, as shown in Fig. 15.

Hardware implementation: To validate the proposed switching algorithm, a 3 kVA direct multilevel matrix converter prototype was developed. The setup consists of a control circuit, CONCEPT gate driver module (6SD106EI), multilevel matrix converter module with bidirectional switches (SEMIKRON-SK60GM123). The control circuit consists of an FPGA (SPARTEN 3A DSP-XC3S1800A) for generating switching pulses for the DTMC.

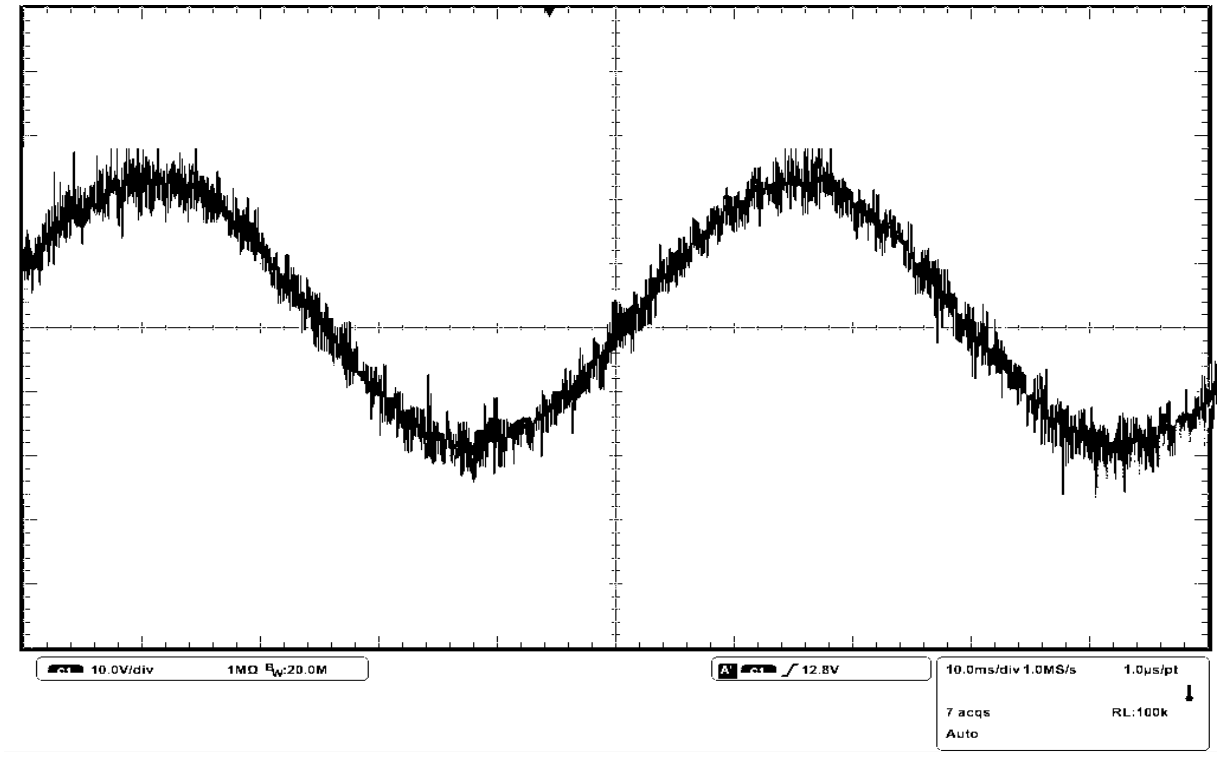
Fig. 16: DTMC hardware prototype



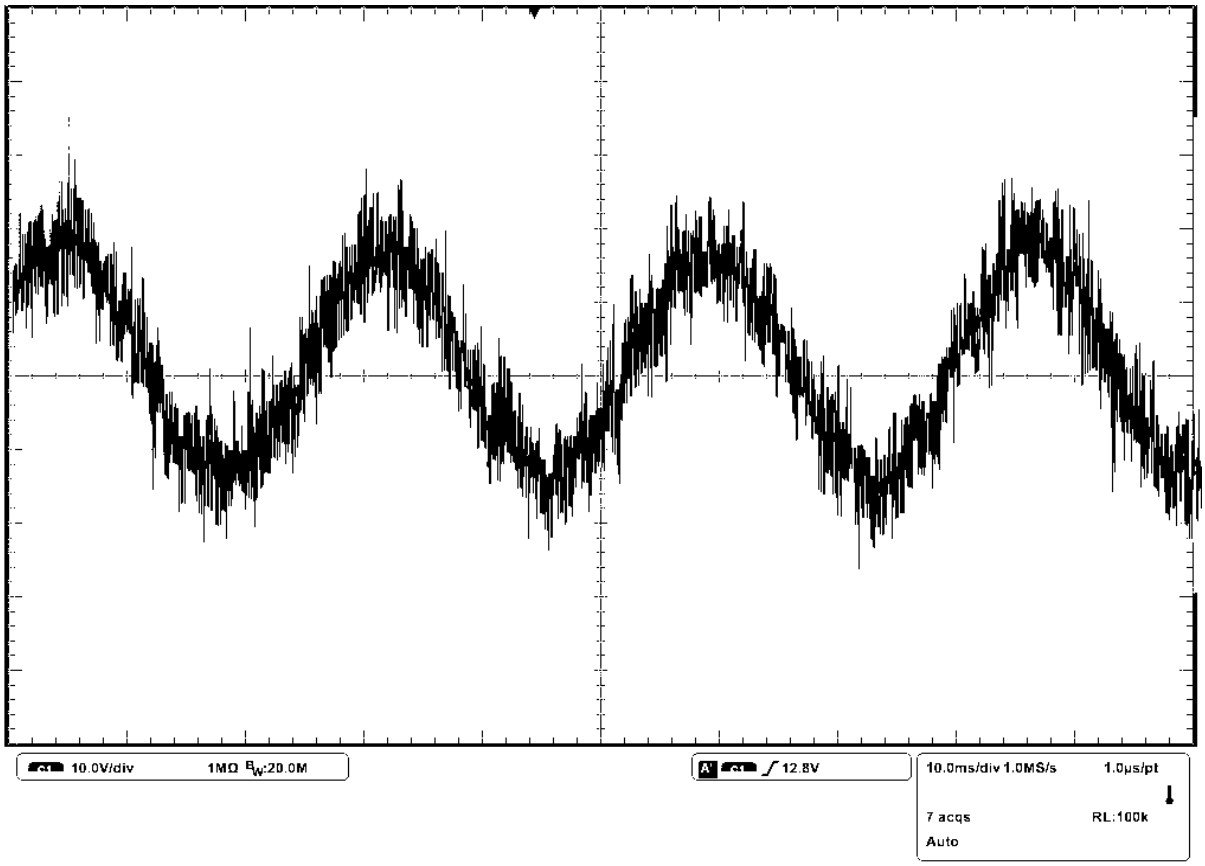
(a)


10.0V/div
1MΩ BW:20.0M
12.8V
10.0ms/div 1.0MS/s
1.0µs/pt
7 acqs
RL:100k
Auto

(b)


10.0V/div
1MΩ BW:20.0M
12.8V
10.0ms/div 1.0MS/s
1.0µs/pt
7 acqs
RL:100k
Auto

(c)



(d)

Fig. 17: Hardware output for balanced input condition (a) output phase voltage, (b) output line voltage, (c) output phase current, (d) input phase current

The switching information and the current direction information were processed using the FPGA for generating the DTMC switching pulses along with the implementation of the four-step commutation. The system generator toolbox in the MATLAB was used to generate the FPGA code in VHDL for generating the firing pulses. The experiment was conducted with a balanced input phase voltage of 100 V, switching frequency of 6 kHz, R_L = 20 Ω, L_L = 21 mH and MI = 0.72. The DTMC was used for converting the 50 Hz input voltage to 25 Hz output voltage. Figure 16 shows the laboratory prototype of the DTMC. Selected waveforms from experimental results shown in Fig. 17 verify the implementation and the effectiveness of the proposed DTMC ISVM method. Figure 17a and b show the output line voltage and the output phase voltage of the DTMC, respectively. Figure 17c shows the 25 Hz output current of the DTMC and Fig. 17d shows the 50 Hz filtered input current of the DTMC.

CONCLUSION

In this study, the space vector PWM technique for the direct three-level matrix converter has been proposed for synthesizing balanced sinusoidal three-level output voltages from balanced and unbalanced non-sinusoidal input voltages. In addition, conduction losses and switching losses were modelled for the DTMC and a comparative study of the same for the CMC and the DTMC has been carried out. MATLAB simulation and hardware results verify the effectiveness of the proposed technique. The THD of the output voltage is lower for the DTMC as compared to the CMC. However, the switching losses for the DTMC are higher than those of the CMC.

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