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Research Article

Modified 16-b Square-root Low Power Area Efficient Carry Select Adder

[1]R.P. Meenaakshi Sundhari and [2]R. Anita
[1]ECE Department, Sasurie College of Engineering, Vijayamangalam, Tirupur District, Tamil Nadu 638056,
[2]Department of EEE, Institute of Road and Transport Technology, Erode, Tamil Nadu 638316, India

Abstract: Due to acceptance of the portable system with fast growth of power density in the integrated circuits, the power dissipation and the performance is considered while the system is designed. The main goal of the VLSI design is to design the adders in more efficient way. By that way the Carry Select Adder (CSLA) is an adder designed, which computes n+1 bit sum of two n bit numbers. In this study Modified 16-b SQRT with Modified Area efficient CSLA is proposed. From the design of Modified Area Efficient CSLA it is experiential that there is an option of reducing the area more and consumes low power when compared with Regular CSLA. Modified Area Efficient CSLA (MA-CSLA) utilizes BEC which reduces the area more and the total gate count is also gets condensed. The proposed study makes use of a simple and well-organized gate-level alteration to considerably reduce the area and power of the CSLA. By the support of alteration 8-, 16-, 32- and 64-b, respectively Square-Root CSLA (SQRT CSLA) model have been evolved and evaluated with the regular SQRT CSLA model. This study estimates the performance of the proposed designs in terms of delay, area and power. The results analysis shows that the proposed Modified Area Efficient CSLA structure is better than the regular SQRT CSLA.

Keywords: Area-efficient, Carry Select Adder (CSLA), delay, modified area efficient CSLA

INTRODUCTION

In VLSI industry, the low power arithmetic circuits are widely used due to fast increase of convenient electronic components. Multiplier-Accumulator (MAC) unit is the major building block in DSP processor. Arithmetic circuits like full Adder is a part of the MAC unit is capable of extensively affect the efficiency of entire system. So for low power application the full adder circuit is essential, because it consumes less power. Carry Select Adder are used for high speed application by dropping the propagation delay (Partha and Debarshi, 2012).

The Carry Select Adder (CSLA) performs parallel computation, which produces additional carriers and limited sum is studied (Bedrij, 1962). The multiplexer is used to select the carry and final sum. In CSLA, Ripple Cary Adders (RCA) with multiple pairs is used though it occupies more area. Hence it is not an area efficient one.

In Bedrij (1962) different systems to progress the complicatedness of carry propagation delay the CSLA is used by autonomously creating several carries and afterward build the sum by selecting a carry.

The fundamental idea introduced by the author is to use Binary to Excess-1 Converter (BEC) as an alternative of RCA with Cin = 1 in the regular CSLA to attain lesser area and power consumption (Ramkumar *et al*., 2010; Ceiang and Hsiao, 1998; Kim and Kim, 2001). The foremost advantage of this BEC logic comes from the smaller number of logic gates than the n-bit Full Adder (FA) construction.

The SQRT CSLA has been selected for relationship with the design as it has a more balanced delay and have need of lower power and area (Rabaey, 2001; He *et al*., 2005).

In this study a Modified 16-b SQRT with Modified Area efficient CSLA is proposed here to reduce the area and power of the CSLA.

LITERATURE REVIEW

In Wang *et al*. (2002) the Ripple carry adder shows the evidence of unsophisticated designs of the circuit but it speed is slow. The Carry Look Ahead adder (CLA) is one of the best one but it occupies large area. CSA is act as a concession between two adders like Ripple carry adder and carry look ahead. In Wang *et al*. (2002) hybrid adders are introduced to speed up the extra process. In Abid *et al*. (2008) a hybrid full adder with low power multipliers is used. Thirty two-Bit Multiplier with a CLA and a 32-bit Multiplier with a RCA are implemented in VHDL to analyze the performance is studied (Krad and Al-Taie, 2008).

Corresponding Author: R.P. Meenaakshi Sundhari, Department of ECE, Sasurie College of Engineering, Vijayamangalam, Tirupur District, Tamil Nadu 638056, India

The author introduced a Carry Select adder (CSL) to reduce the delay as compared with the other existing adders. This adder has a deepness of knowledge in logarithmic gate to design any of the formation an adder's family. The Ripple-Carry Adder (RCA) is used in CSL which leads to less performance. So one of the fastest adder called Carry Select Adder (CSLA) is used to carry out the arithmetic operation as earlier. The CSLA is a best adder that provides optimal result in VHDL execution and it may effectively diminish the CSLA parameters. The simulation result shows that the modification 32-b CSLA (CSLA) structural design gives better result as compared with the other techniques is studied in Shalemraju *et al*. (2012).

In Cadence (2008) the author presents a Square-Root CSLA (SQRT CSLA) which reduces the area and the power as it is compared with the other techniques to evaluate the performance.

METHODOLOGY

The basic adder circuits and the proposed methodology is described as follows.

Basic adder block: By the help of basic adder block, this section explains how to calculate the area and the delay also that it shows the effects of the both during implementation. The AND, OR and Inverter (AOI) execution of an XOR gate is shown in Fig. 1. The delay and area estimation method consist of the each gates are made by AND, OR and Inverter comprises of delay equal to 1 unit and area equal to 1 unit. Later add up the amount of gates in the greatest path of a logic block that provides the maximum delay. The area evaluation is done by counting the total number of AOI gates requisite for each logic block.

Binary to Excess-1 Converter (BEC): Binary to Excess-1 Converter (BEC) used in the regular CSLA to accomplish lesser area and the execution speed gets enlarged. This logic is restored in RCA with Cin = 1. This logic can be executed for unlike bits which are used in the adapted design. The major benefit of this BEC logic comes from the truth that it uses minor number of logic gates than the n-bit Full Adder (FA) arrangement. Since confirmed on top of the main idea of this study is to use BEC as an alternative of the RCA with Cin = 1 in order to decrease the area and raise the speed of process in the regular CSLA to get modified CSLA. Toward restore the n-bit RCA, an n+ 1 bit BEC logic is needed. The structure of 6-bit BEC is shown in Fig. 2.

Architecture of modified 16-bit SQRT CSLA: The Modified 16-Bit SQRT CSLA is analogous to regular 16-bit SQRT CSLA, the only change is that, replace RCA with Cin = 1 among the two accessible RCAs in a group with a BEC. This BEC has a characteristic that it can carry out the similar operation as that of the restore RCA with Cin = 1. Figure 3 shows the Modified block diagram of 64-bit SQRT CSLA. Compared to RCA the

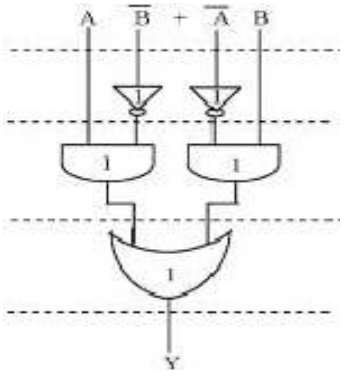


Fig. 1: Delay and area evaluation of XOR

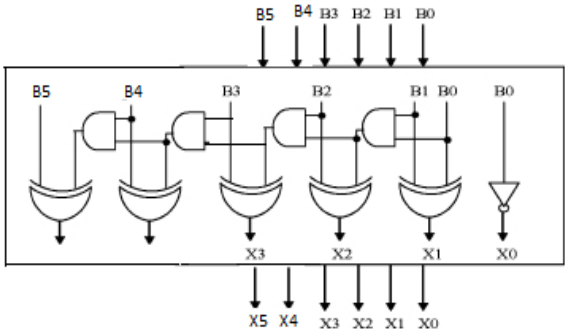


Fig. 2: 6-binary to excess-1 converter

BEC logic needed one extra bit. The block diagrams in which it may separate into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and analogous mux. As in the Fig. 4, Group 0 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum (1:0) and carry out which is acting as mux selection line for the next group, likewise the process carry on for higher groups but they contain BEC logic as an alternative of RCA with Cin = 1. Based on the concern of delay values, the arrival time of selection input C1 of 6:3 mux is former than the sum of RCA and BEC. Intended for left over groups the selection input arrival is later than the RCA and BEC. Therefore, the sum1 and c1 (output from mux) depends on mux and results calculated by RCA and BEC correspondingly. The sum 2 depends on c1 and mux. Intended for the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

Proposed method for delay and area evaluation for modified 16-bit SQRT CSLA with modified area efficient CSLA: The Modified 16-bit SQRT CSLA is linked with the RCA and its operation is studied before. The most important design of MA-CSLA is to use 4 gates XOR which lessen the total number of gate count.

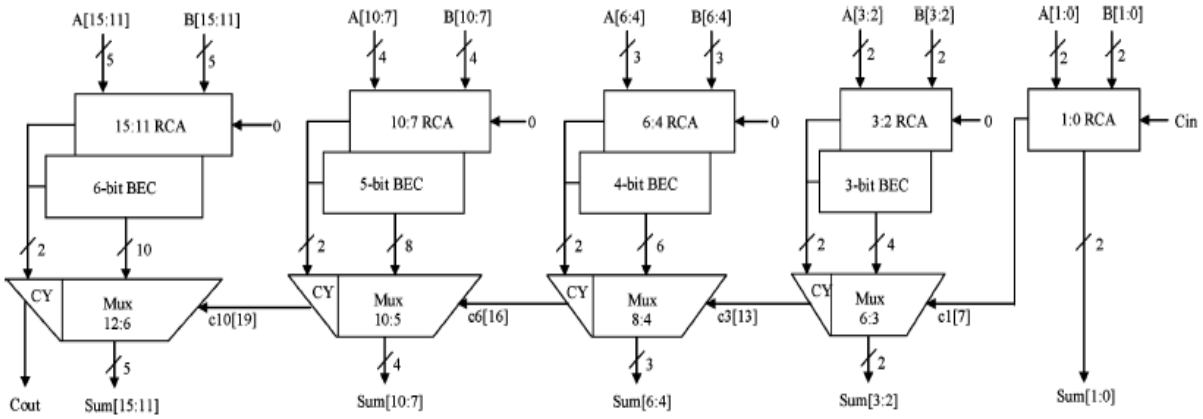


Fig. 3: Architecture of modified 16-bit SQRT CSLA

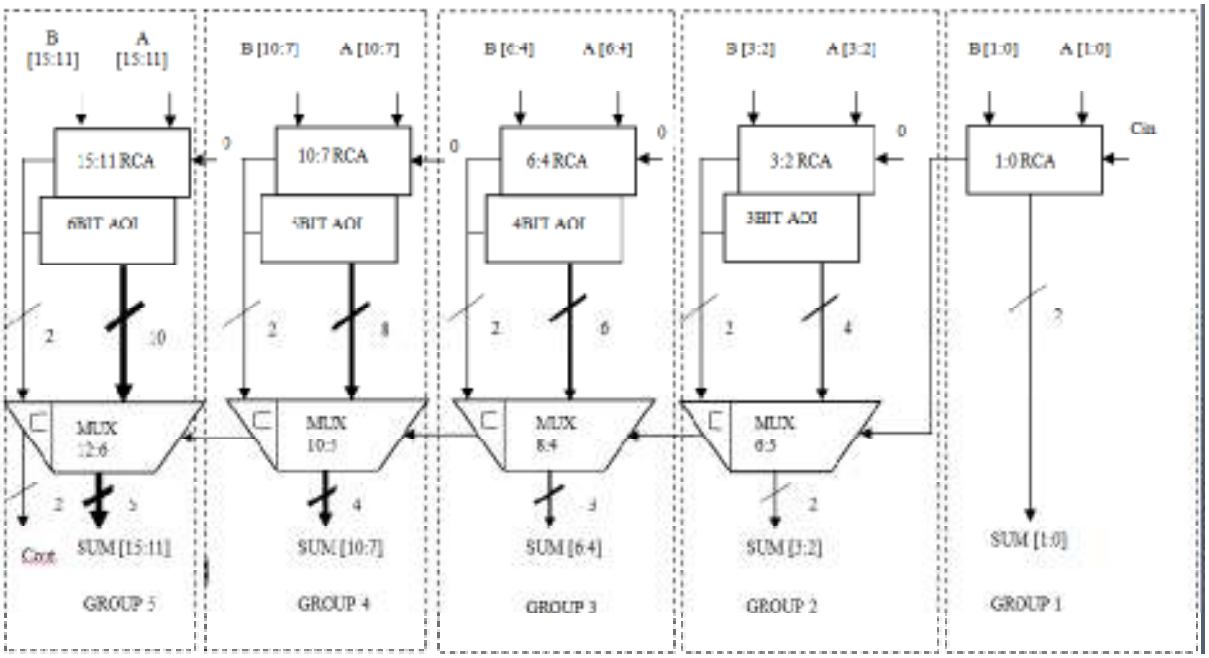


Fig. 4: Modified Area efficient Carry Select Adder (MA-CSLA)

From the Fig. 4 it is obvious that there is the likelihood of reduction of gates by means of using the XOR gates which has been proposed in the design. In the Modified CSLA the total number of XOR gates is considered to be 210. In Modified Area efficient CSLA (MA-CSLA) which consist of less number of XOR gates is 168. The below expression is used in the Modified Area efficient CSLA (MA-CSLA) for an XOR operation:

$$Y = (a + b)(\sim ab)$$

The formation of the proposed Modified 16-b SQRT CSLA using BEC for RCA with Cin = 1 is to optimize the area and power. The structure of 16 bit Modified Area efficient CSLA (MA-CSLA) is shown in the Fig. 4 and the area valuation of each group is shown in Fig. 4. The group 2 has one 2-b RCA which has 1 FA and 1 HA for Cin = 0. As an alternative of another 2-bit RCA with Cin = 1 a 3 bit AOI is used which adds one to the output.

The proposed Modified 16-bit SQRT CSLA with Modified Area Efficient CSLA is shown in the Fig. 5. The gate count for group2 is as follows:

Group 2:
FA = 11 (11*1)
HA = 5 (5*1)
BEC = 9 (NOT = 3 and = 4, OR = 2)
MUX = 12 (3*4)

Similarly, the gate counts for other groups are determined.

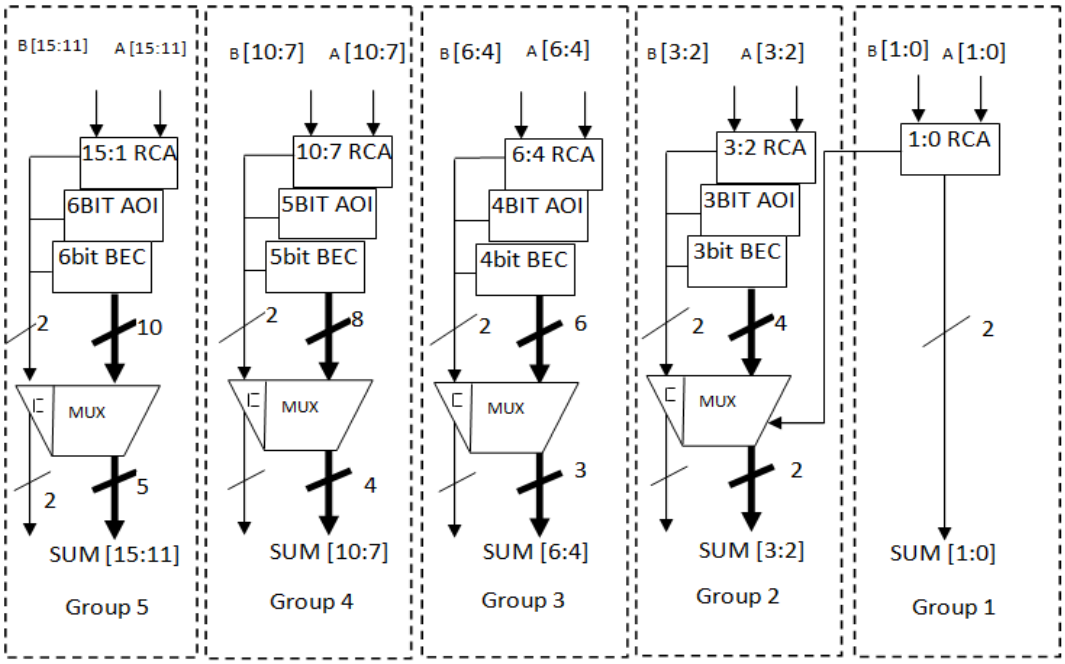
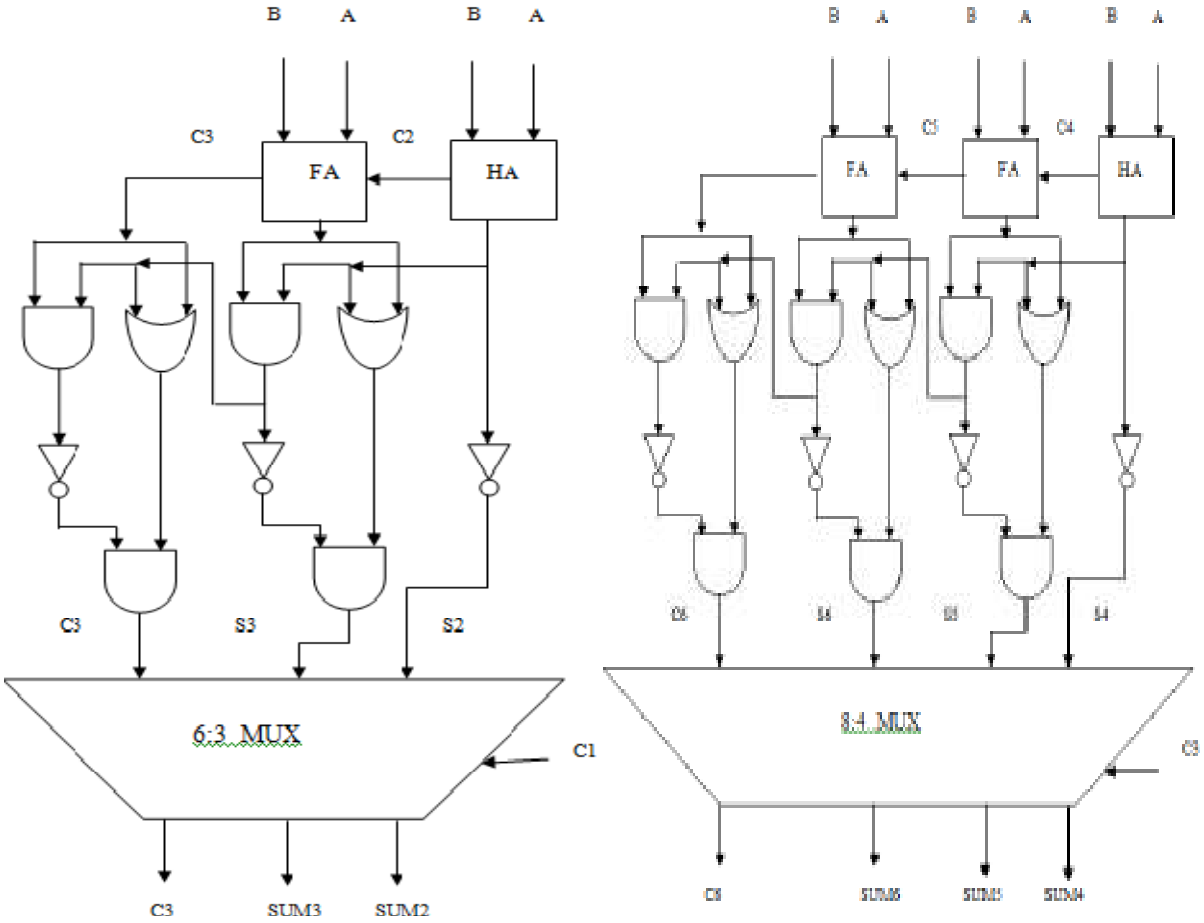
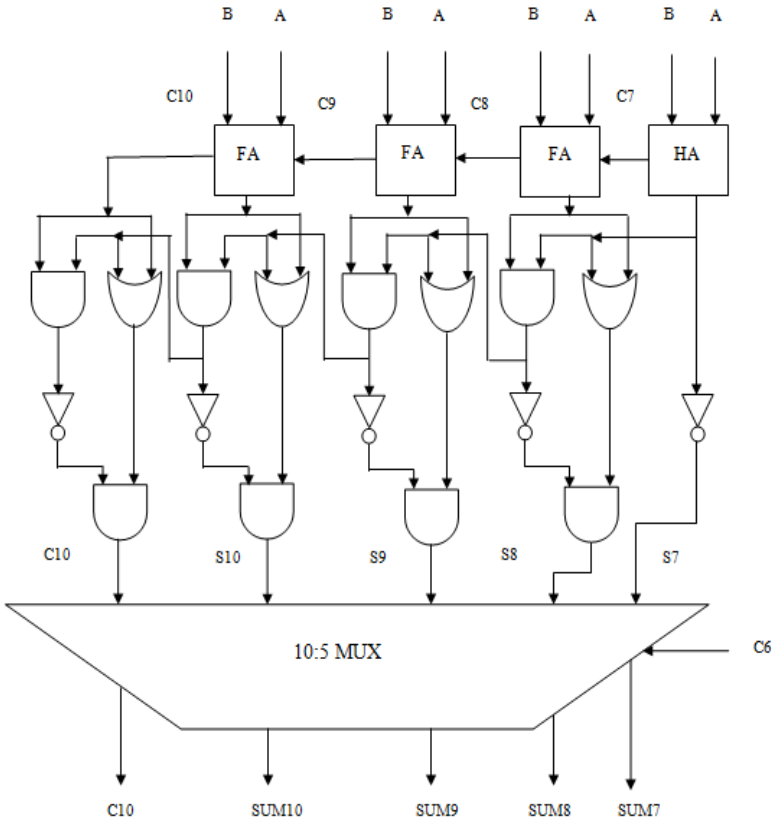
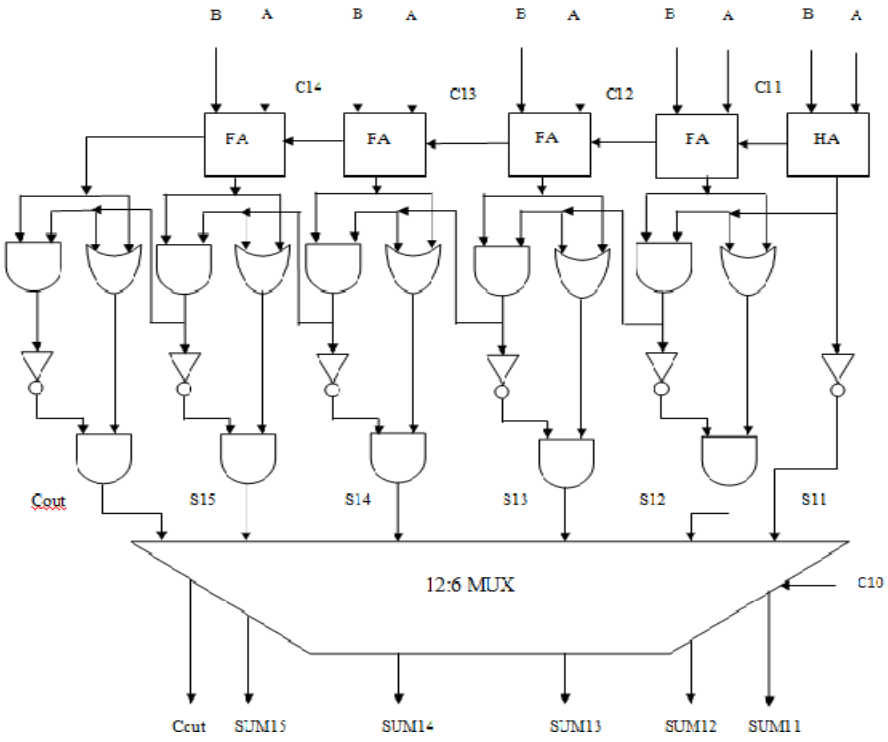


Fig. 5: Proposed modified 16-bit SQRT CSLA with modified area efficient CSLA





(c)



(d)

Fig. 6: (a): Group 2; (b): group 3; (c): group 4; (d): group 5

Table 1: Delay comparison

Group	Delay for SQRT CSLA	Delay for MSQRT MCSLA
Group 1	17.434	13.624
Group 2	7.422	6.683
Group 3	8.652	6.810
Group 4	8.907	6.108
Group 5	11.451	10.696

Table 2: Power comparison

Group	Power based on SQRT CSLA	Power based on MSQRT MCSLA
Group 2	0.887	0.813
Group 3	0.887	0.876
Group 4	1.454	1.450
Group 5	1.731	1.451

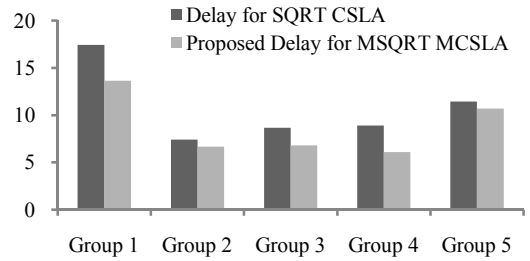


Fig. 7: Delay comparison

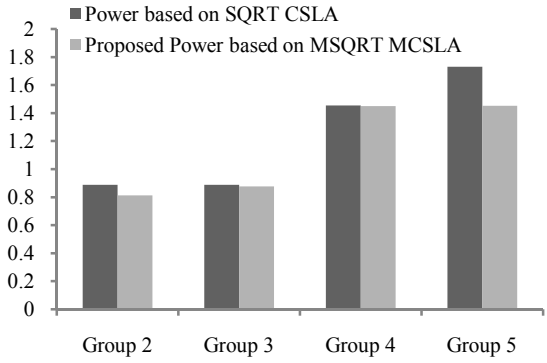


Fig. 8: Power comparison

In Fig. 6a, It is verified that when C1 = 0 the 2 bit sum arrives from RCA. When C1 = 1 the 2 bit sum arrives from BEC.

In Fig. 6b to d the operation of group 3 to 5 is shown.

ASIC IMPLEMENTATION RESULTS

The proposed design used in this research study has been developed using Verilog-HDL and synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology. The synthesized Verilog netlist and their respective Design Constraints file (SDC) are imported to Cadence SoC Encounter and are used to generate automated layout from standard cells and placement and routing (Cadence, 2008). Parasitic extraction is performed using Encounter's Native RC extraction tool and the extracted parasitic RC (SPEF format) is back annotated to Common Timing Engine in Encounter platform for static timing analysis.

The performance of the proposed approach is evaluated using the performance metrics such as Delay comparison and power comparison.

Table 1 exhibits the simulation results of both the CSLA structures in terms of delay.

Table 1 and Fig. 7 show the delay comparison for existing SQRT CSLA approach and the proposed MSQRT MCSLA approach. It is observed from the table that the proposed approach provides lesser delay when compared with the existing approach. The percentage reduction in the cell delay is observed to be significant. For group 1, the percentage of reduction is 21.85%, where as group 2, 3, 4 and 5, the percentage of reduction in delay is 9.95, 21.28, 31.42 and 6.59%, respectively.

Table 2 shows the power comparison for existing SQRT CSLA approach and the proposed MSQRT MCSLA approach. It is observed from the table that the proposed MSQRT MCSLA approach consumes lesser power when compared with the existing approach. The percentage reduction in the power consumption is observed to be significant as shown in Fig. 8. For group 2, the percentage of reduction is 8.34%, where as group 3, 4 and 5, the percentage of reduction in delay is 1.24, 0.27 and 16.17%, respectively.

The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power. The percentage reduction in the cell area and total power as function of the bit size are shown in Fig. 9. Similarly, percentage reduction in power-delay product and the area-delay product are shown in Fig. 10.

It is clear that the area of the 8-, 16-, 32- and 64-b proposed SQRT CSLA is reduced by 9.7, 15, 16.7 and 17.4%, respectively. But, for the proposed MSQRT MCSLA approach, the area of the 8-, 16-, 32- and 64-b, is reduced by 8, 12, 14 and 16%, respectively.

Similarly for power, it is clear that the power of the 8-, 16-, 32- and 64-b proposed SQRT CSLA is reduced by 7.6, 10.56, 13.63 and 15.46%, respectively. But, the proposed MSQRT MCSLA approach outperforms the SQRT CSLA approach with reduced power consumption of 6, 9, 12 and 13.3% for the bit sizes 8-, 16-, 32- and 64, respectively.

The delay overhead also exhibits a similarly decreasing trend with bit size. The delay overhead of the existing SQRT CSLA for the 8, 16 and 32-b is 14, 9.8 and 6.7%, respectively, whereas for the 64-b it reduces to only 3.76% as shown in the Fig. 11. However, the proposed approach shows better delay overhead reduction when compared with the existing work. The proposed MSQRT MCSLA reduces the delay overhead by 11, 7, 5.3 and 3.3% for 8, 16, 32 and 64-b, respectively.

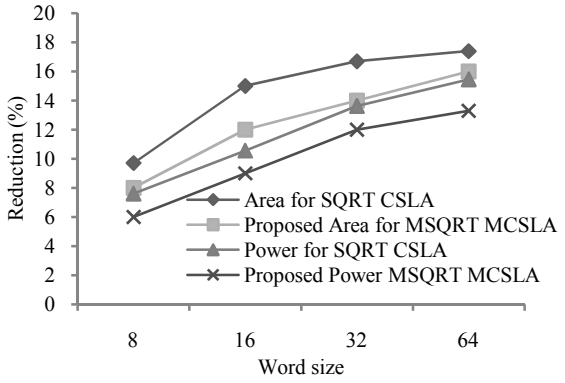


Fig. 9: Percentage reduction in the cell area, total power

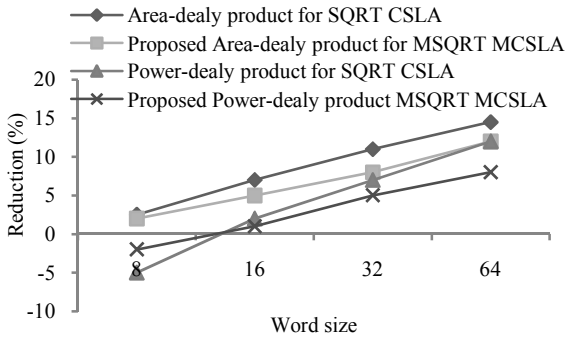


Fig. 10: Percentage reduction in the power-delay product and area-delay product

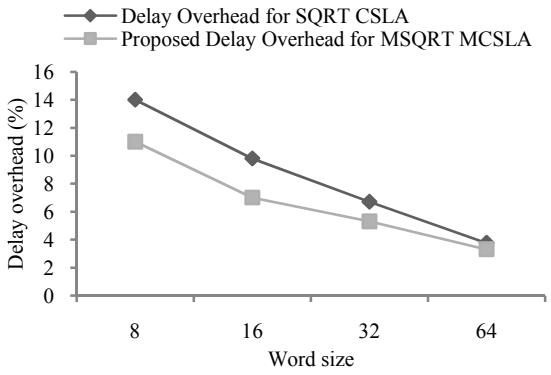


Fig. 11: Percentage reduction in of delay overhead

CONCLUSION

In this study Modified 16-bit SQRT with Modified Area Efficient CSLA is proposed to reduce Low-Power and Area. The compact structure is formed while reducing the number of gates of this study gives the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a somewhat bigger delay but the area and power of the 64-b modified SQRT CSLA are considerably reduced. The power-delay creation and the area-delay creation of the proposed design show a decrease for 16-, 32- and 64-b sizes, respectively which point out the accomplishment of the method and not a simple exchange of delay for power and area. Therefore the proposed Modified 16-bit SQRT with Modified Area Efficient CSLA show the achievement of attaining low area, low power, simple and well-organized for VLSI hardware implementation.

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