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Research Article

Performance Analysis of Mixed Carrier-pulse Width Modulation Scheme

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Abstract: This study deals with the performance analysis of Pulse Width Modulation (PWM) scheme for three phase voltage source inverter though intermingling of multiple carriers. The proposed PWM scheme using two groups of carriers (inverted Sine wave and Triangle wave), each group having carrier and its 90° shifted. The arbitrary selection of these carriers is based on the linear feedback shift registers value ('0' or '1'). This random carrier selection is serving to improve the spectral quality of the output of the inverter. This improved waveform has been derived from third harmonic injected sine PWM technique. Simulation results confirm the effectiveness of the proposed scheme in providing very less harmonic noises with minimum distortion and satisfactory fundamental component. This study also shows the implementation compatibility of the work with Field Programmable Gate Array environment.

Keywords: Harmonic spread factor, linear feedback shift register, pseudo random binary sequence, random pulse width modulation, voltage source inverter

INTRODUCTION

Various deterministic frequency pulse width modulation schemes have been recently proposed for three phase Voltage Source Inverters (VSI) (Lim *et al*., 2010). Essentially, most of the attempts adopt the sinusoidal pulse width modulation and space vector approach to solve the problem of higher dc bus utilization, lowest total harmonic distortion (Kim *et al*., 2009; Boopathi *et al*., 2012). These PWM schemes are using deterministic switching frequency causes discrete frequency harmonics, electromagnetic interference and acoustic noise. Two major causes of the audible acoustic noise problems are the motor structure and PWM schemes employed by the inverters. The audible switching noise problem can be minimized by increasing the switching frequency of the switching devices up to 20 kHz, but this type of increased switching frequency schemes evidences to highest switching losses of the inverter (Lim *et al*., 2010; Kim *et al*., 2009).

Any kind of modulation in PWM is either through the modification of the shape of the carrier and the shape of the reference. The pseudo random triangular carrier modulation schemes have been investigated (Lim *et al*., 2010; Kim *et al*., 2009), these PWM schemes are based on the use of non-deterministic random number have been proposed to generate random PWM waveforms for AC drives. When the randomness added into the PWM waveform, it causes the harmonic power to spread over the harmonic spectrum, so that there is no harmonic component has a significant magnitude (Hui *et al*., 1995). Inverted sine carrier has been discussed (Nandhakumar and Jeevananthan, 2007; Seyezhai and Mathur, 2009), as a part of carrier modification to improve the fundamental component in the inverter output.

In this study, it deals with the performance analysis of pulse width modulation schemes for three phase voltage source inverter though intermingling of multiple carriers. The carriers have been grouped based on their shape, one is triangle and another one is inverted sine. Each group having two carriers, triangle and inverted sine and its 90° shifted. So, four carriers have been employed and the selection is based on Pseudo Random Binary Sequence (PRBS) bits. This approach is based on the logical operation of several bits of a digital number and is commonly known as pseudo PWM code generator in communications. By first doing some logical operations on selected bits, a new bit value is obtained. By shifting the number by one bit with the new bit forming the most significant bit, a new number is then generated (Hui *et al*., 1995). Two eight bit linear feedback shift register based PRBSs have been used. The combination of the triangle carrier and sine inverter is leading to the new role of both harmonic power distribution and the fundamental improvements.

Field programmable Gate Arrays (FPGAs) have become one of the most popular implementation media for digital circuits and their preamble in 1984 (Gayathri and Chandorkar, 2008). The main difference from DSP

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and microprocessor-based solutions is that FPGAs allow concurrent operation (simultaneous execution of all control procedures), enabling high performance and computational, making the implementation of intensive control methods feasible. The advent of FPGA technology has made many computational intensive PWM strategies in reality (Sreekanth and Moni, 2013). The proposed pulse generation scheme is designed by using very high speed integrated circuits hardware description language (VHDL) for the digital circuit implementation (Stephen *et al*., 2012). The crucial success of FPGAs is their programmability which allows any circuit to be instantly composed out by appropriate programming. The Three phase inverter is designed in MATLAB environment. With the use of HDL co-simulator tool box in MATLAB, three phase inverter switches capture the pulses generating from Modelsim FPGA simulator tool.

PROPOSED RANDOM PULSE GENERATION SCHEME

In the proposed random carrier system composed of four carrier generation each of same fixed frequency, two linear feedback shift registers and a 4×1 MUX in the digital implementation shown in Fig. 1. LFSRs are made up of XOR gates which are used to generate the two PRBS random pulses. LFSR tapping points are 4, 5, 6 and 8th bits are used to perform XOR gate operation. The initial value of the two registers are different to avoid, to get the same value of bits. These random pulses decide the resultant carrier by using a 4×1 mux, which is going to compare reference wave as shown in Table 1. The interaction points of the reference and carrier wave decides the switching frequency of the power switches.

Table 1: Carrier selection based on PRBS1 and PRBS2 signal

PRBS1	PRBS2	Resultant carrier
0	0	Triangle
0	1	Sine
1	0	90° Shifted sine
1	1	90° Shifted triangle

3 kHz switching frequency have been selected because of the tradeoff between switching loss by the power device and harmonics impact of the output magnitude.

The digital implementation of the reference wave which is Third Harmonic Injected Sinusoidal PWM (THIPWM) generation have been focused to utilize very less FPGA resources with improved speed and power consumption. Figure 2 shows that the reference wave implementation circuit. In this implementation only 50 sine sampling data have been used to generate first quadrant sine reference wave. 2nd, 3rd and 4th quadrant reference waves are generating from first quadrant as per mathematical formulae (1), (2) and (3):

$$\sin(90^o + \theta) = \sin 90^o - \sin\theta \quad (1)$$

$$\sin(180^o + \theta) = -\sin\theta \quad (2)$$

$$\sin(270^o + \theta) = -(\sin 90^o - \sin\theta) \quad (3)$$

Sampling interval of the sine data retrieved from memory is 1.8°. Modulator reference signal (V_{ref}) have been generated as per Eq. (4):

$$V_{ref} = Ma(sinw_m t + \left(\frac{1}{3}\right) sin3w_m t; \quad 0 \le w_m t \le 2\pi \quad (4)$$

For implementation, two multipliers and one adder have been used.

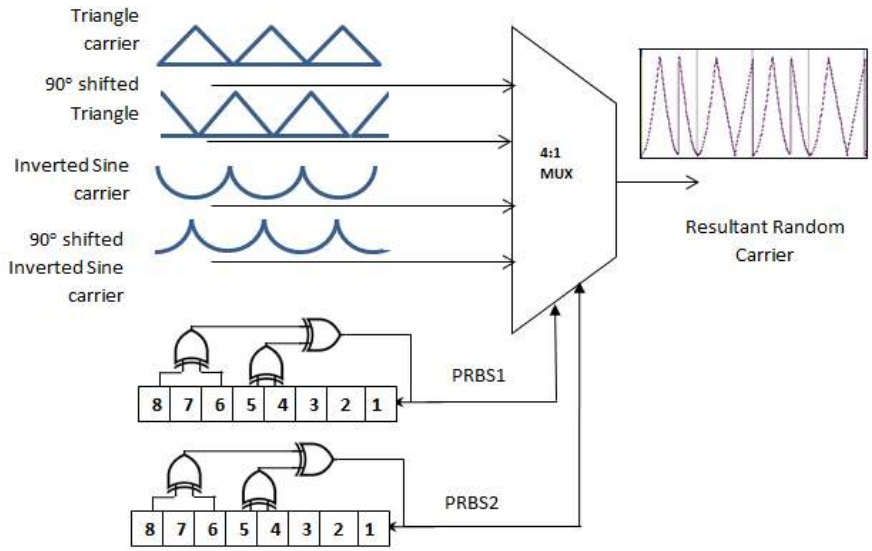

Fig. 1: Proposed random carrier generation

RESULTS AND DISCUSSION

Harmonic Spread Factor (HSF) is the performance evaluation indicator to investigate the acoustic noise of the PWM based induction motor drives (Lim *et al*., 2010; Boopathi *et al*., 2012). The concept of statistical deviation is employed for HSF calculation for evaluating the harmonic spread effect of the random PWM. The HSF can be defined as follows:

$$HSF = \sqrt{\frac{1}{N}\sum_{j>1}^{N}(H_j - H_0)^2} \quad (5)$$

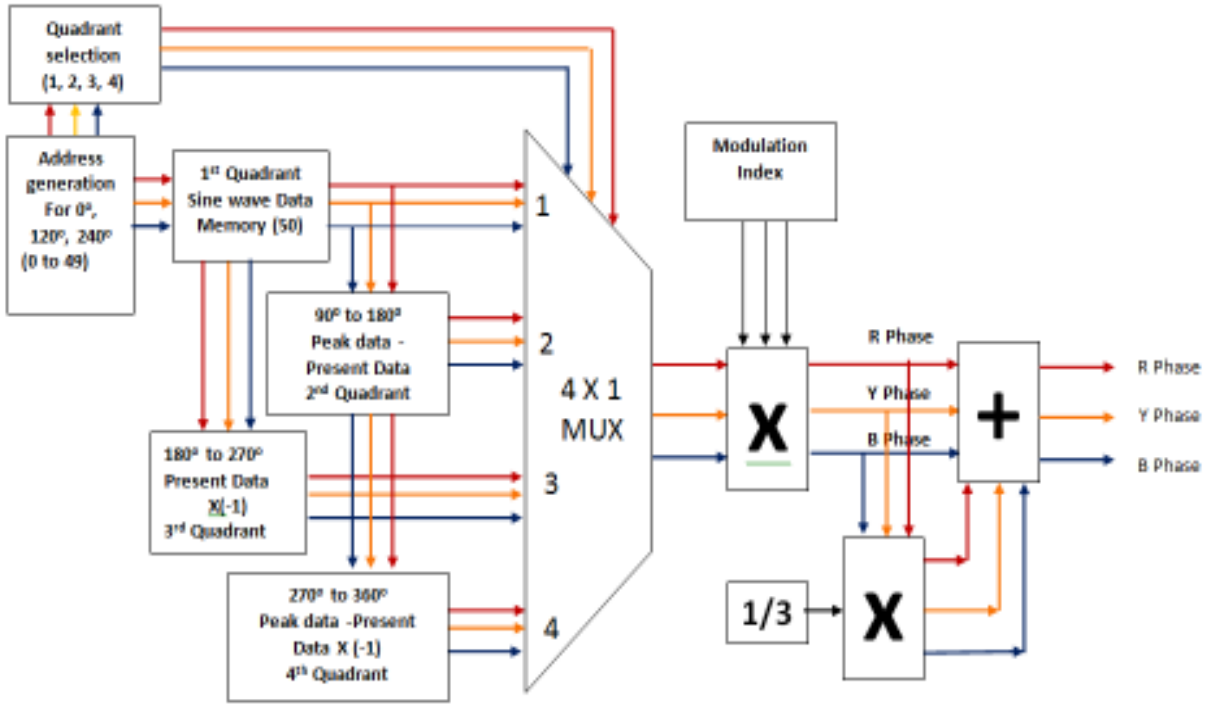

Fig. 2: Proposed reference wave generation

Table 2: Performance indices of conventional and proposed schemes

		PWM Techniques		
Ma	Performance parameters	SPWM	Two triangle RPWM	Proposed mixed carrier RPWM
0.2	Fundamental	37.76	36	34.79
	THD	253	258	268.78
	HSF	3.57	3.3	7.27
0.4	Fundamental	75.6	74	65.65
	THD	163	164	180.04
	HSF	4.79	4.46	5.42
0.6	Fundamental	113	112	103.6
	THD	119	123	130
	HSF	5.38	4.78	4.17
0.8	Fundamental	150.3	151	136.5
	THD	93.6	93	103.1
	HSF	5.49	4.56	3.23
1	Fundamental	188.6	189	176.9
	THD	80.63	81.53	76.39
	HSF	4.49	3.83	2.32

Table 3: Dominating harmonic order (D-H-O) and its amplitude for Ma = 0.8

Conventional schemes				Proposed scheme	
SPWM		Random triangle PWM		Mixed carrier PWM	
D-H-O	Va	D-H-O	Va	D-H-O	Va
58	45	119	62	120	46.5
62	42	121	51	118	42.29
119	61	239	21	89	12.11
121	51	120	19	124	11.88

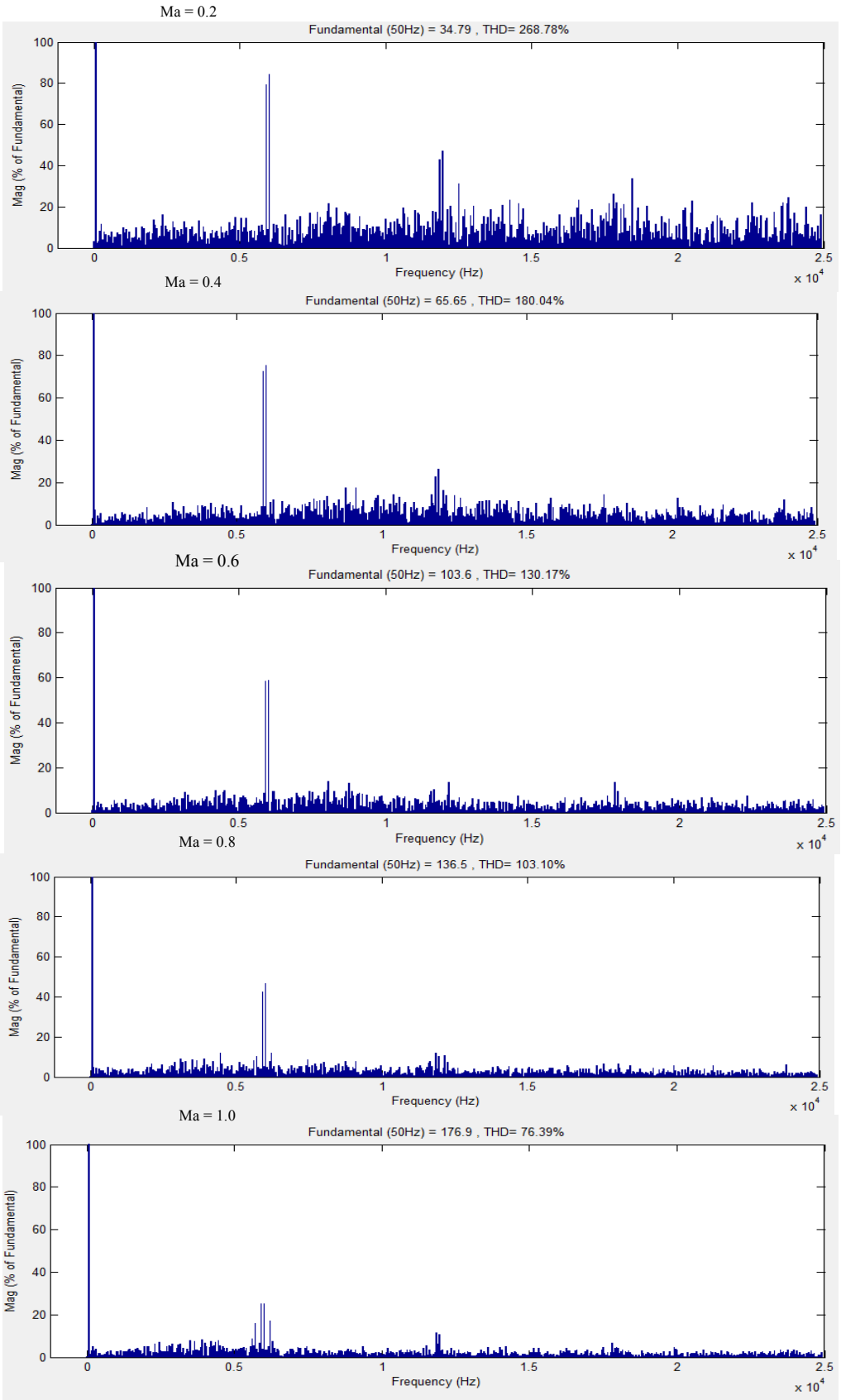

Fig. 3: Line to line voltage spectrum from Ma = 0.2 to 1.0 (V_{dc} = 220 V)

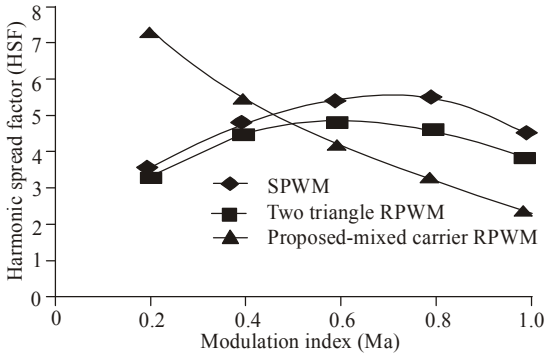

Fig. 4: Harmonic spread factor comparison of conventional and proposed scheme

$$H_0 = \sum_{j>1}^{N}(H_j)/(N-1) \quad (6)$$

where, 'H_j' is amplitude of jth harmonics, 'H_0' is average value of all 'N' harmonics. The HSF quantifies the harmonic spectra spread effect of random PWM scheme and it should be small. For an ideally flat spectrum of white noise, the HSF would be zero.

Proposed scheme have been simulated by using three phase voltage source inverter with 220 V_{dc}. Figure 3 shows that the line to line voltage spectrum of modulation index (Ma) from 0.2 to 1.0. The evaluation chart has been given for various modulation index (Ma) ranges from 0.2 to 1.0 shown in Table 2. In Table 3, gives the evaluation chart for Dominating Harmonic Order (D-H-O) and its amplitude value for Ma = 0.8. The peak amplitude of the dominating harmonic is 46.5 V, but its order is 120 (6 kHz), whereas peak magnitude order of the harmonic is 58 (2.9 kHz) in SPWM and 119 (5.95 kHz) in Two Triangle RPWM scheme.

Figure 4 and Table 2 and 3 clearly depicts that peak amplitude of the dominating harmonic is very less when compared with the conventional schemes.

FPGA COMPATIBILITY

The scheme has been design by using VHDL language for FPGA device environment. Modelsim based digital simulation results of carrier and reference wave generation are shown in Fig. 5 and 6. Resultant RPWM pulses are shown in Fig. 7 with Ma = 1.0 and fs = 3 kHz. This has been synthesized by using Xilinx13.1 project navigator tool.XC3S500E FG320-4, 90 nm technology FPGA device has been selected for synthesis.

Interestingly, this multiple carrier PWM digital work has occupied only 26% of the slices of FPGA resources. 6 DSP based multipliers have been used to

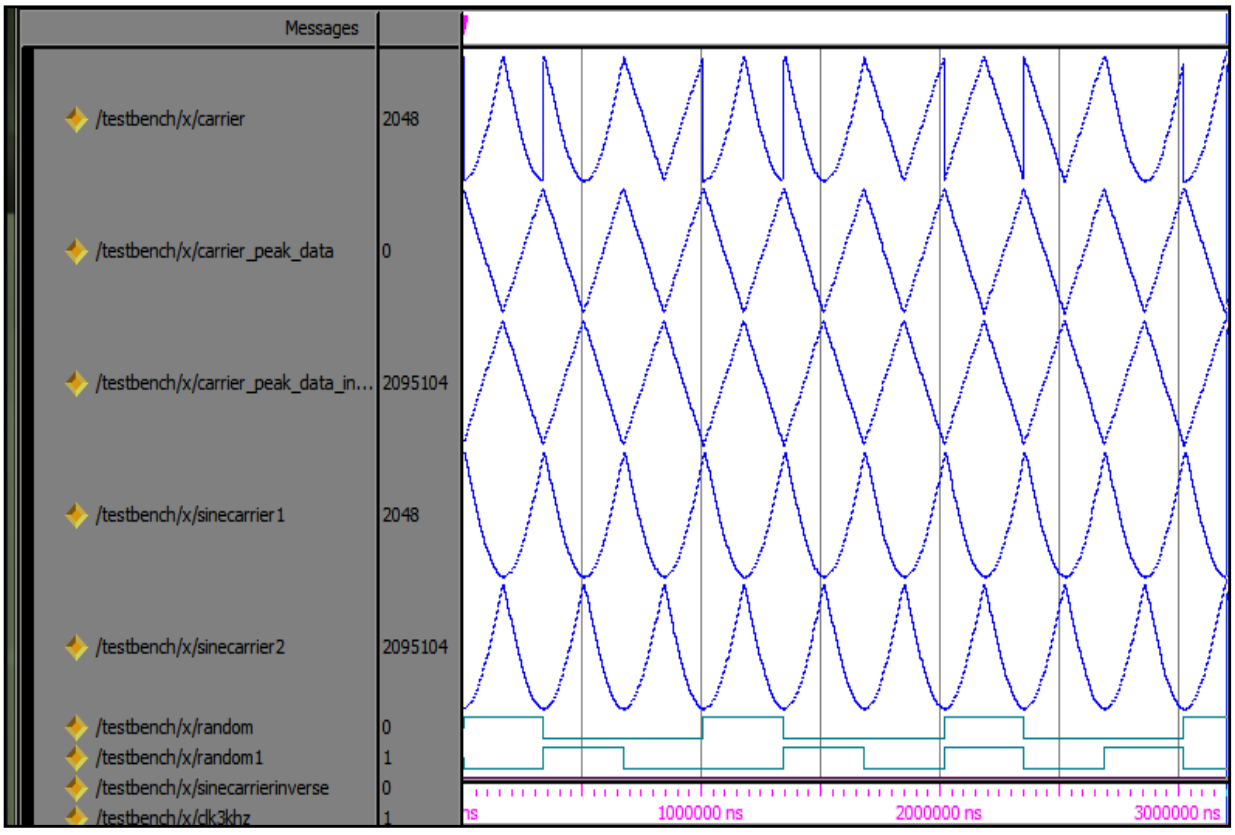

Fig. 5: Simulation output of the carrier generation (f_s = 3 kHz)

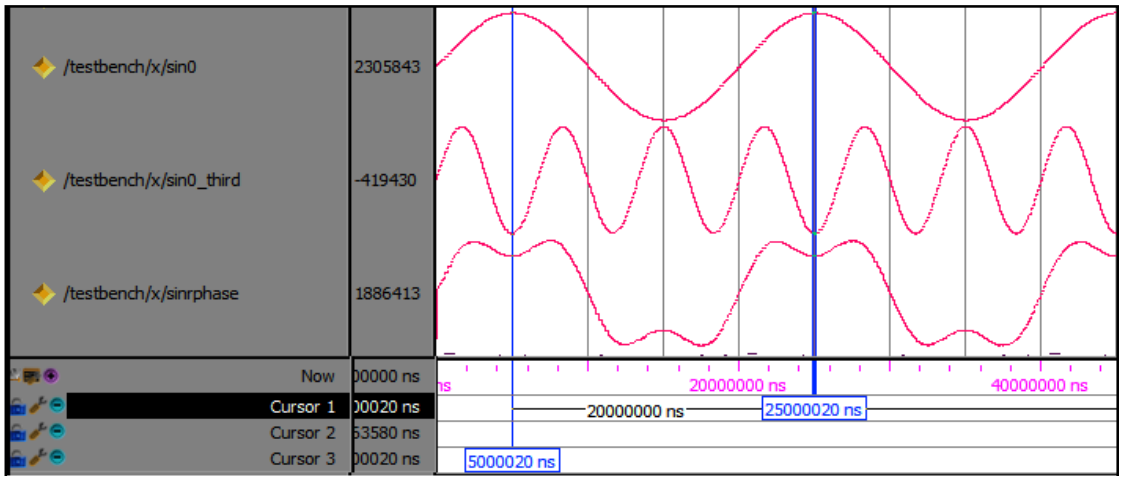

Fig. 6: Simulation output of the reference generation (V_{ref} = 50 Hz)

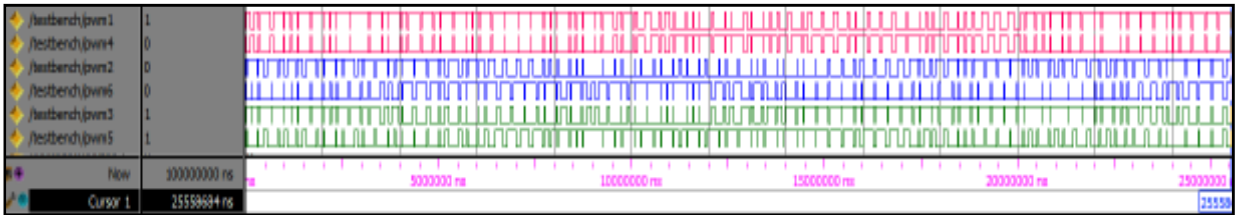

Fig. 7: Simulation results of the RPWM pulses (Ma = 1.0)

Table 4: FPGA device resource utilization

Device utilization summary (estimated values)

Logic utilization	Used	Available	Utilization
Number of slices	1211	4656	26%
Number of slice flip flops	783	9312	8%
Number of 4 input LUTs	2315	9312	24%
Number of bonded IOBs	8	232	4%
Number of MULT18X18SIOs	6	20	30%
Number of GCLKs	4	24	16%

Timing summary:

Speed grade: -4
Minimum period: 15.980 ns (Maximum frequency: 62.578MHz)
Minimum input arrival time before clock: 7.059 ns
Maximum output required time after clock: 4.283 ns
Process "Synthesize - XST" completed successfully

generate the THIPWM shown in Table 4. 50 MHz clock oscillator has been used for sequential circuits. A Xilinx power estimator tool is used to estimate power analysis. Device static power or quiescent power is a function of process voltage and temperature. In this study, static power dissipation is 78 mW. Dynamic power dissipation is 30 mW. Total power dissipated by FPGA device is 108 mW.

CONCLUSION

The mixed carrier with third harmonic injected sinusoidal PWM scheme is presented. This digital control pulse generation scheme is simple to design and implement by FPGA device for three phase VSI. Figure 4 shows that the critical performance comparison of conventional and mixed carrier scheme. Figure 3 and 4 clearly depicts that the significant reduction of the harmonic spread factor which decides the acoustic noise of the motor for the Modulation index above 0.4 with the satisfactory performance reduction of fundamental and total harmonic distortion. This scheme is applicable in industries to provide noiseless environment.

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