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Research Article

High Speed Reconfigurable FIR Filter using Russian Peasant Multiplier with Sklansky Adder

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Abstract: The Reconfigurable FIR filters are commonly used digital filters which find its major applications in digital signal processing and multi-standard wireless communications. The Direct form of FIR filter used in DSP application which consumes more area and power. To overcome this problem Multiplier Control Signal Decision (MCSD) window schemes is incorporated into direct form FIR filter in order to dynamically change the filter order. Conventional reconfigurable FIR filter is designed using Russian Peasant Multiplier which consumes more area and delay due to poor performance of adder used in multiplication unit. In this study, modified reconfigurable FIR filter is designed to further reduce the area, power and time. In proposed Reconfigurable FIR filter, a Wallace adder is replaced by carry select adder with sklansky adder in Russian Peasant Multiplication technique. Hence, modified Reconfigurable FIR filter with carry select adder with sklansky adder consumes less area, delay and power than the conventional Reconfigurable FIR architecture with Russian Peasant Multiplication technique.

Keywords: Carry save adder, FPGA, MCSD scheme, modified reconfigurable FIR filter, Russian peasant multiplier, sklansky adder

INTRODUCTION

Finite Impulse Response (FIR) filters are widely used as an effective tool in Digital Signal Processing (DSP) and Multimedia applications. It requires the two main factors known as low complexity and reconfigurability. The major factor of filter complexity is depends on the adders performed in multiplication unit. In the other hand, reconfigurability of FIR filter realizes the filter performance during determining the filter order. The fundamental of input-output relationship of the Linear Time Invariant (LTI) FIR filter can be expressed as following Eq. (1):

$$y(n) = \sum_{k=0}^{N-1} c_k \, x(n-k) \quad (1)$$

where, N denotes the length of FIR filters, c_k represents the filter coefficients and x (n-k) represents the time-shifted input data samples. In many applications, in order to attain the high spectral suppressions and/or noise reduction, FIR filter with moderately huge number of tabs are essential. Many prior efforts focus on the optimization of the filter coefficients whereas maintaining a filter order (Gustafson, 2007). In those approaches, reducing the number of adder/subtract or add and shift unit is one of the main goal for research. Even, one of the drawbacks in those approaches is that once the filter architecture is designed, the coefficients cannot be altered. Therefore, these approaches cannot be used for programmable coefficients. In Chen and Chiueh (2006) according to the stop band energy of the input signal, the filter order is dynamically changed. But, the approach affects the slow filter order adaptation time due to energy calculations in the feedback mechanism. In Previous studies (Ludwig *et al*., 1996) show that reducing the both input data samples and filter coefficients prior to convolution operation has desired energy quality features of FIR filter. Structural Reconfigurable FIR filter designs are previously proposed in Yu *et al*. (2001) for low power implementations and to realize the frequency response by using a single filter (Mahesh and Vinod, 2008, 2010). For low power FIR filter architectures, number of input word-lengths and filter taps, different coefficients word length and dynamic reduced signal representations are widely used. In those works, the large overhead is incurred to support the reconfigurable schemes. Lee *et al*. (2011) Multiplier Control Signal Decision window (MCSD) technique is incorporated into Reconfigurable FIR filter for attain low power and high speed applications. This method is mainly used for dynamically change the filter order. But area and delay consumption is more in those approaches. The Constant Elimination Method (CEM) is proposed for selecting the filter coefficients in Ramkumar *et al*. (2013). The pipelined booth multiplier is replaced to trade off the

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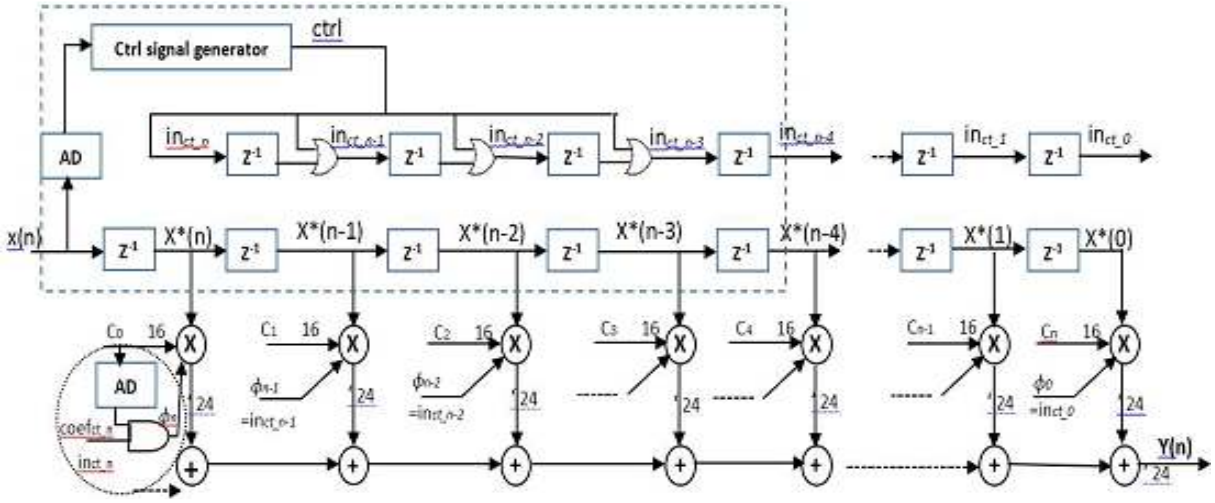

Fig. 1: Block diagram of reconfigurable FIR filter using MCSD technique

filter performance for dynamic power utilization is proposed in Sriram and Selvakumar (2013). The Vedic multiplier is used in reconfigurable FIR filter consumes less area when compared to the proposed architecture in Lee *et al*. (2011). The booth multiplier is replaced by Vedic multiplier in reconfigurable FIR filter for low power and high speed applications. In previous analysis, the Russian peasant multiplier is used in reconfigurable FIR filter is proposed. It offers good performance when compared to the Vedic multiplier. But, adder unit used in that model performs more delay and complexity of the circuit is increased.

In our study, the Reconfigurable FIR filter is modified by using carry select adder with sklansky adder instead of Wallace adder used in Russian Peasant multiplier to optimize the area, delay and power utilization. This modified Reconfigurable FIR filter offers less area and delay when compared to the conventional Reconfigurable FIR filter designed by Russian Multiplier. Simulation for proposed reconfigurable FIR filter is performed by ModelSim6.3c and Synthesis is carried out by xilinx10.1.

METHODOLOGY

Reconfigurable FIR filter: The architecture for reconfigurable FIR filter by using Multiple Control Signal Decision (MCSD) window (Lee *et al*., 2011) is shown in Fig. 1. This structure continuously adapt the amplitude of input samples for removes the right multiplication process. The Amplitude Detector (AD) is used to detect the input sample of x (n). The Amplitude Detector circuit depends on the input threshold where the fan-in's of AND and OR gate are determined by a comparator circuit. If x (n) is smaller than the threshold, the output of AD is set to '1'. The amplitude of input samples are abruptly changes for every cycle, the multiplier will be turned on and off continuously which considerably produce switching activities. To solve the switching problem MCSD technique is used in Fig. 1. In MCSD, ctrl signal is used to count the consecutive input samples which are slighter than threshold and multiplier is turned off only when consecutive input samples are lesser than threshold. When the counter detect the consecutive input samples slightly than threshold, then the ctrl signal changes to '1' which indicate that successive low amplitude input samples are detected and multipliers are ready to turn off. One additional bit is added in dotted line of Fig. 1 is controlled by ctrl signal. Multiplier is used to multiply the input sample with coefficient.

Figure 1 performs the filter operation but different configuration is shown for reducing the area, delay and power consumptions.

Conventional Russian peasant multiplier: A novel Russian Peasant Multiplication is introduced by Russian. The Russian Peasant Multiplier architecture (Yu and Meher, 2014) consists of shifters, 2:1 Multiplexers and adder unit. It is a simple architecture which consumes less area and delay for computations of multiplications. When compared to the Vedic multiplier, Russian Peasant Multiplier provides less APT (Area, Power and Time) product. Architecture of the 8-bit Russian Peasant Multiplier is shown in Fig. 2. Similarly, 16-bit Russian Peasant Multiplier can be extended from 8-bit Russian Peasant Multiplier. Shifters and Multiplexers in Fig. 2 are used to perform the partial product operations which consume less area and power than Vedic multiplier. For addition of partial product carry save adder is used in Fig. 2 represented as Wallace adder. Further to reduce area and delay, carry select adder with sklansky adder is used instead of Wallace adder in Russian Peasant Multiplier architecture which explained in next section. To reduce the switching activity, control signal generator circuits are used in MCSD window.

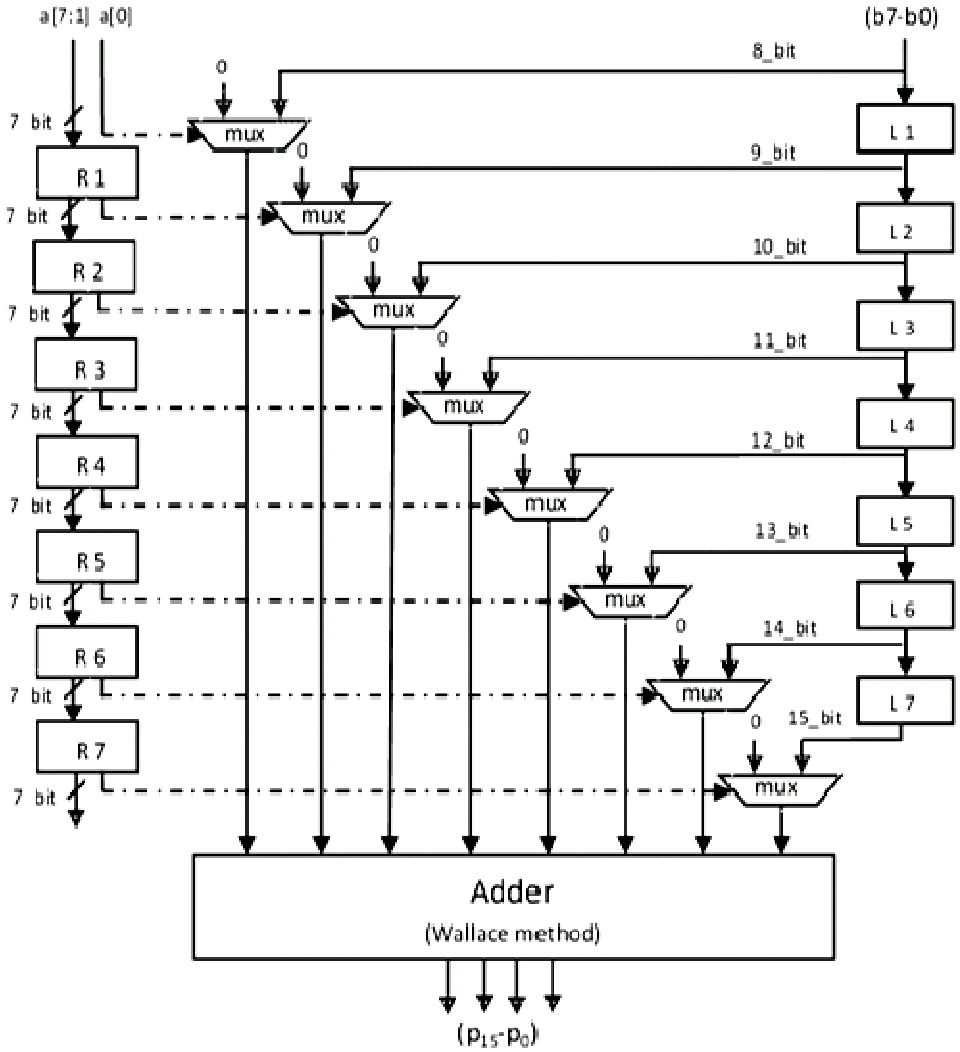

Fig. 2: Architecture of 8-bit Russian peasant multiplier

Proposed Russian peasant multiplier with sklansky adder: The Reconfigurable FIR filter is mostly used for various DSP applications and multi-standard wireless communications. Reconfiguration technique is used for fixed coefficient as well as programming coefficient values. The complexity of reconfigurable FIR filter is founded in multiplication unit. In conventional reconfigurable FIR filter, the Russian Peasant multiplier is used for performing Multiplications. In Russian Peasant Multiplier architectures, two type of shifters namely 'L' and 'R' indicated as left shifter and right shifter respectively are used. This performs shifting operations and consecutive 2:1 multiplexers are used to select valid bits as partial products. Each LSB of right shifter is used as the selection signal for each multiplexer. Finally, the partial products are added by using carry save adder which consists of Ripple Carry Adder (RCA) and number of one bit full adders unit. The adder unit in Russian Peasant Multiplication results in large delay and area. In order to reduce the area and delay of the Multiplication, carry save adder is replaced by carry select adder with sklansky adder in our proposed work. In carry select adder, dual RCAs used for performing addition operations. Generally RCA consumes more area and delay due to carry propagation. In order to reduce the delay, dual RCAs can be replaced by One RCA and one Binary to Excess1 converter this architecture named as SQRT CSLA.

Further, reduce the delay in CSLA; the upper part of RCA can be replaced by sklansky adder in our proposed work. Sklansky adder is one of the fast parallel adders for performing addition operation with less delay. The Multiplier architecture with carry select adder using sklnsky adder is shown in Fig. 3.

RESULTS AND DISCUSSION

Simulation for existing Russian Peasant Multiplier with carry save adder and proposed Russian Peasant

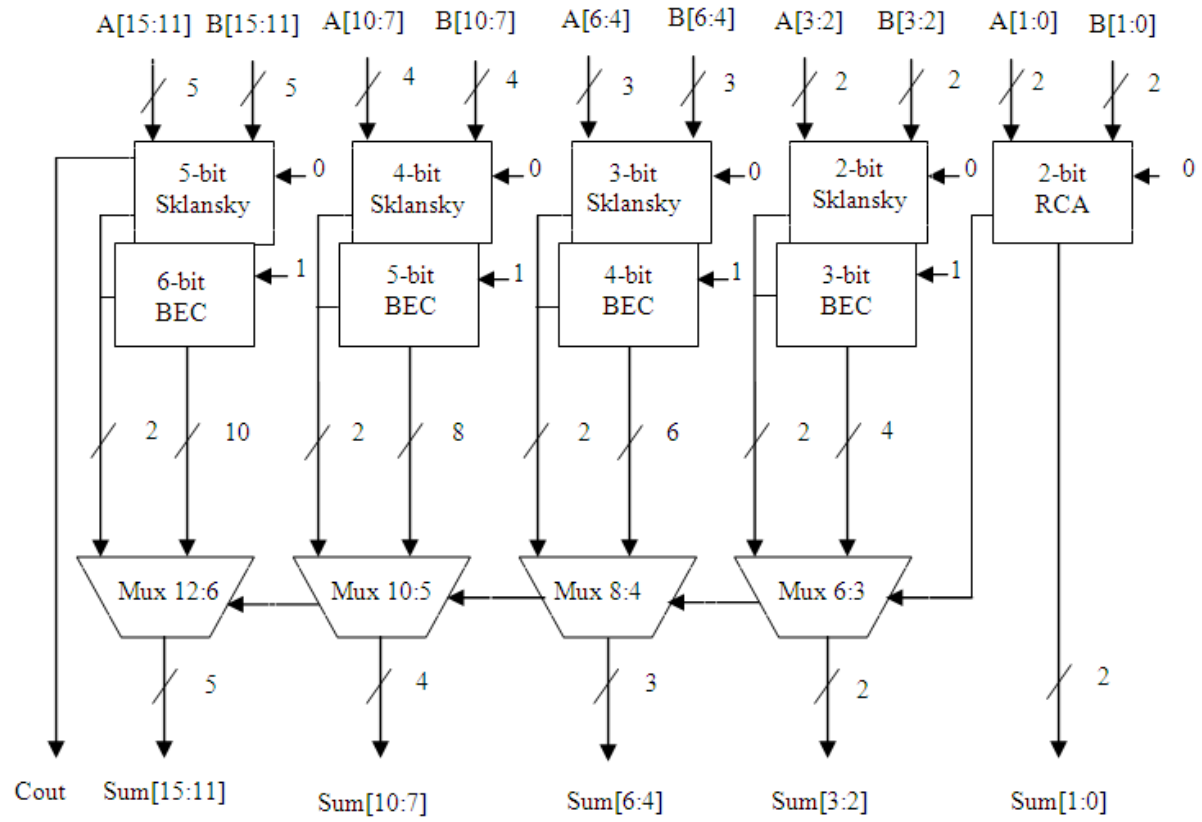

Fig. 3: Proposed carry select adder using sklansky adder

Table 1: Comparison between 24-bit carry save adder and 24-bit carry select adder with sklansky adder

Method	Delay (nsec)	Area
24-bit carry save adder	41.252	45
24-bit carry select adder with sklansky adder	25.354	38

Table 2: Comparison of different adder with Russian peasant multiplier

Method	Delay (nsec)	Area
Russian peasant multiplier with carry save adder	52.376	371
Russian peasant multiplier with carry select adder using sklansky adder	36.196	371

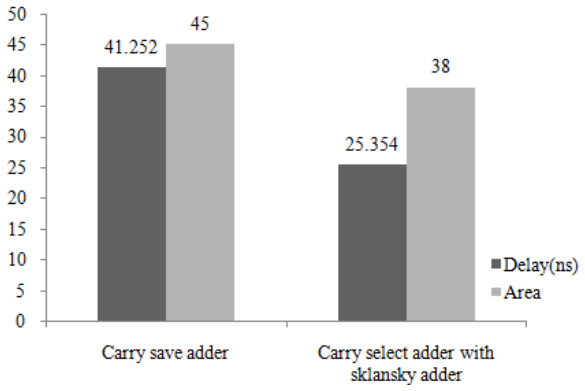

Fig. 4: Performance analysis for carry save adder and carry select adder with sklansky adder

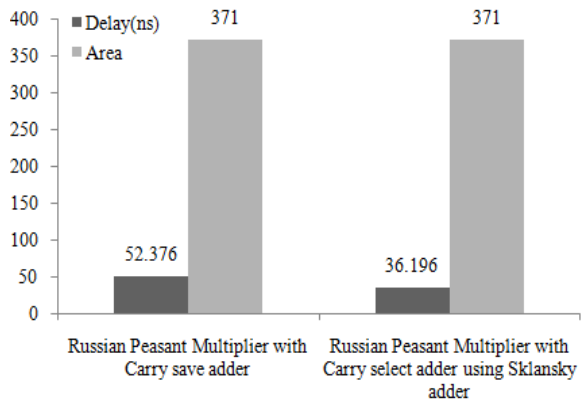

Fig. 5: The performance analysis for different adder with Russian peasant multiplier

Multiplier with sklansky adder has been designed using Verilog HDL and implemented in a Xilinx Spartan 3 XC3S200 (package: pQ208, speed grade: -5) FPGA using the Xilinx ISE 10.1i design tool. The performance of delay and area for 24-bit carry save adder and 24-bit

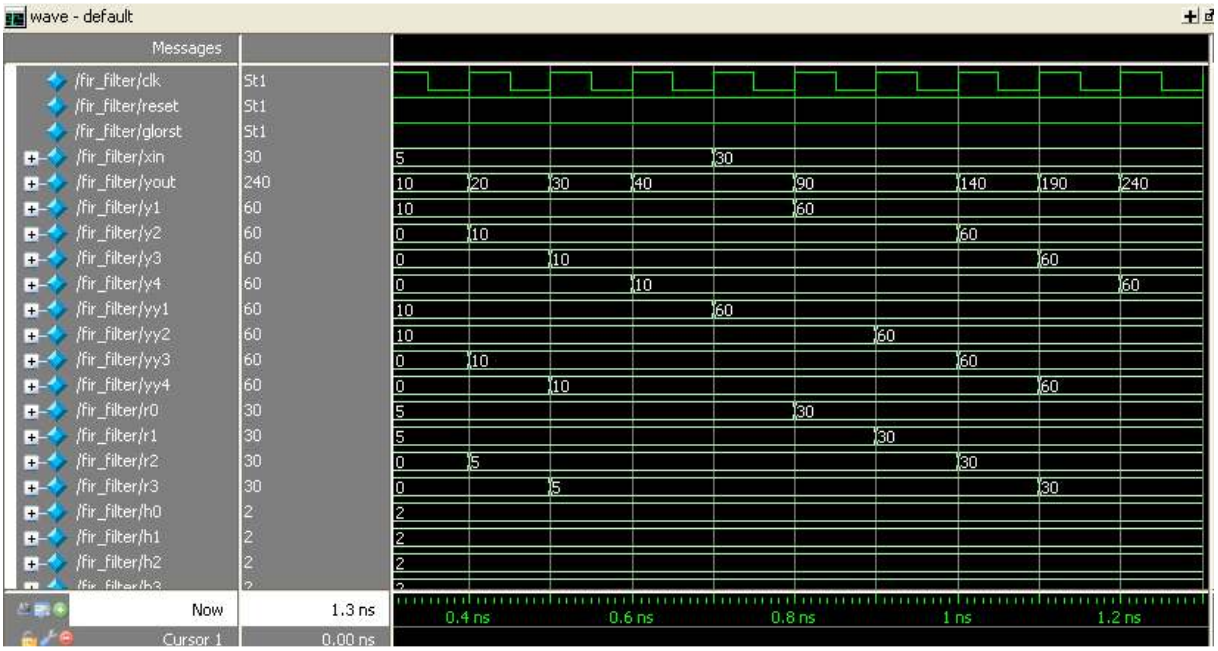

Fig. 6: Simulation result of proposed reconfigurable FIR filter with Russian peasant multiplier using carry select adder with sklansky adder

carry select adder with sklansky adder is analyzed and compared in Table 1.

Table 1 show that the carry select adder with sklansky adder consumes less area and delay when compared to the carry save adder. The performance analysis for existing and proposed adder is as pictorial diagram shown in Fig. 4.

It shows that, 15.5% area reduction and 38.5% delay reduction is achieved in carry select adder with sklansky adder when compared to the conventional carry save adder. Further the delay for multiplier can be reduced by replacing the carry select adder with sklansky adder instead of carry save adder in Russian Peasant Multiplier. The Performance between Russian Peasant Multiplier with carry save adder and Russian Peasant Multiplier with carry select adder with sklansky adder is shown in Table 2.

From the comparison for different adder used in Russian Peasant Multiplier, the delay is reduced, when carry select adder with sklansky adder is incorporated with Russian Peasant Multiplier than the conventional Russian Peasant Multiplier. The performance for different multiplier is represented as pictorial diagram is shown in Fig. 5.

From the comparisons, 30.9% area reduction is achieved in Russian Peasant Multiplier with carry select adder using sklansky adder than the conventional Russian Peasant Multiplier. It shows that better utilization of area and delay when using the sklansky adder for performing addition in multiplier.

The Proposed high performance Russian Peasant multiplier is incorporated into reconfigurable FIR filter and results are analyzed in Verilog HDL (Hardware Description Language). The functionality of this simulation is measured using modelsim 6.3c and the utilization of area and delay for the filters are measured by synthesis process in Xilinx10.1i tool. Simulation result of proposed reconfigurable FIR filter with Russian Peasant Multiplier with carry select adder using sklansky adder is shown in Fig. 6.

CONCLUSION

In this study, an area efficient and high speed Russian Peasant Multiplier is modified by replacing the carry select with sklansky adder instead of carry save adder used in multiplier. The proposed Russian Peasant Multiplier offers 30.9% delay reduction compared to the conventional Russian Peasant Multiplier. The modified Russian Peasant Multiplier is incorporated with reconfigurable FIR filter. This proposed reconfigurable FIR filter with modified Russian Peasant Multiplier is compared with the conventional reconfigurable FIR filter with Russian Peasant Multiplier. The result shows that the proposed reconfigurable FIR filter offers less area and power reduction than the conventional reconfigurable FIR filter. In future, the proposed FIR filter is applied in multi-standard wireless communication and image processing application.

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