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Research Article

A Comprehensive Evaluation of Drain-side Layout Topologies on the Power nLDMOS ESD/LU Reliabilities

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Abstract: The non-uniform turned-on and low holding-Voltage (V_h) issues are seriously impacted the reliability abilities of an n-channel lateral-diffused power MOSFET (nLDMOS). Therefore, basing on the drain Field-Oxide Device (FOD) structure of an nLDMOS and changing the thin-Oxide Definition (OD) topology for contacts located in the middle region of drain-side will be investigated in this study. The OD structure will renew as some dotted-OD manners. Experimental results show that the dotted-OD layout has a higher Electrostatic Discharge (ESD) capability than that of the FOD structure and the layout type of dotted-OD will affect the ESD capability of an HV component. A uniformly distributed type of dotted-OD will have a highest I_{t2} value, the I_{t2} value is increased about 12% as compared with the Ref. traditional nLDMOS. And, the V_h value will increase with the contacts number increasing within the dotted-OD, which is increased about 28.2% of a dotOD46 device as compared with the traditional nLDMOS. Furthermore, as adding an FODs structure combined with a uniform dotted-OD structure in the drain side will be haven a high ESD capability (about 5.9% increasing) and high LU immunity (25.8% increasing) compared with the traditional nLDMOS DUT. Therefore, it is good both for ESD and Latch-Up (LU) reliability considerations.

Keywords: Electrostatic Discharge (ESD), Field-Oxide Device (FOD), holding Voltage (V_h), n-channel Lateral-Diffused MOSFET (LDMOS), Oxide Definition (OD), secondary breakdown current (I_{t2}), trigger Voltage (V_{t1})

INTRODUCTION

It is well known that an n-channel Lateral-Diffused power MOSFET (nLDMOS) has been commonly used as the output driver or ESD device in a high-voltage circuit for its low on-resistance and fully compatible with the existing CMOS technologies. Therefore, it is well suited for applications in electronic power-switch components, power management ICs, automotive electronics, LED illuminations, LCD drivers, communication modules, broadband wireless power amplifiers and RF power stations (Zhou *et al*., 2011; Choi *et al*., 2012; Sagneri *et al*., 2013). And, the High-Voltage (HV) power devices have become more and more important. However, an nLDMOS has several serious shortcomings, including a multi-finger type device can't completely turn on which will result in the Electrostatic Discharge (ESD) capability per unit length is very weak and the holding Voltage (V_h) value is very low as compared with the supply voltage VCC_{max}. Meanwhile, the operating voltage of an HV device is very high which indeed need a more better reliability (Kohno *et al*., 2004; Walker *et al*., 2009; Salman *et al*., 2012; Qian *et al*., 2013). An nLDMOS is still a surface dominated MOSFET structure and most of the on-state conduction in an nLDMOS flows along the silicon surface and high electric field around silicon surface accelerated the impact ionization phenomenon. Nevertheless, nLDMOS transistors are inherently frail with respect to ESD/LU stress and enhancing their ESD/LU immunities have been an on-going target (Jeon *et al*., 2002; Chen and Ker, 2009, 2010; Chen *et al*., 2009, 2010; Lee *et al*., 2010; Shrivastava and Gossner, 2012). Many efforts to enhance the ESD or LU capability of an HV MOSFET are usually concerned with improving reliability in the source end (Chen and Ker, 2009; Chen *et al*., 2009; Chen and Wu, 2013; Chen *et al*., 2013), n-well (Chen and Lee, 2014), NBL (Lee *et al*., 2007) and embedded SCR structure (Lee *et al*., 2002; Chen and Ker, 2011; Chen *et al*., 2011; Griffoni *et al*., 2011; Huang *et al*., 2013). However, does there have any other potential solutions? If an HV nLDMOS is added with an FOD and OD engineering in the drain side, will the ESD reliability be enhanced?

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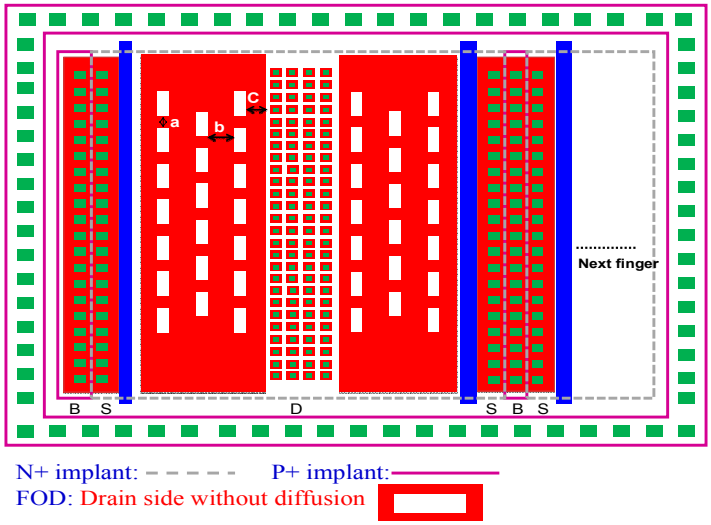

Fig. 1: Schematic layout of an HV nLDMOS with adding FODs and a dotted-OD structure in the drain-side, where the dotted-OD is uniform distributed and one contact involved

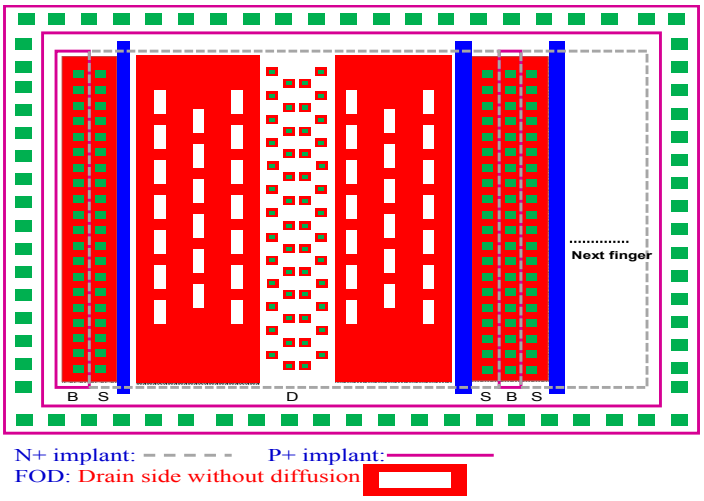

Fig. 2: Schematic layout of an HV nLDMOS with adding FODs and a dotted-OD structure in the drain-side, where the dotted-OD is discrete gap distributed and one contact involved

SAMPLES AND METHODS

Preliminarily, adding the FODs structure in the drain-side of an HV nLDMOS is regarded as a basic architecture in this study. Then, changing the contacts layout of an OD region in the drain-side makes the OD layout renew as the dotted-OD types as shown in Fig. 1 to 4. As a result, the ESD clamp ability of these new nLDMOS DUTs will be carried out in this study. All test DUTs for this work are fabricated by a TSMC 0.25-µm BCD 60-V process. Then, a multi-finger structure of gate-grounded n-channel MOS (GGnMOS) will be used, the channel Length (L) of each finger nLDMOS is kept to be 2-µm, channel Width (W_f) of each finger nLDMOS is 100-µm and total channel Width (W_{tot}) is kept a constancy, 600-µm. Meanwhile, the stripe number (M) a multi-finger structure in these LDMOS DUTs is 6.

Here, the main target of this study is to modulate the layout topologies and to vary the location of contacts in the drain side and which will result in changing the series resistance and eventually achieving a uniform conducting. Therefore, layout parameters of FODs were fixed (column # of FODs is fourteen; the length by width of an FOD is 3×0.6 µm; a = 0.6-µm, b = 0.6-µm, c = 0.54-µm) shown in Fig. 1. The parameter "a" is the spacing distance between one FOD block and next one FOD block in the same column of FODs; the parameter "b" is a distance between the nearest parallel FOD columns; and the parameter "c" is a distance between the nearby FOD edge to the drain-contact

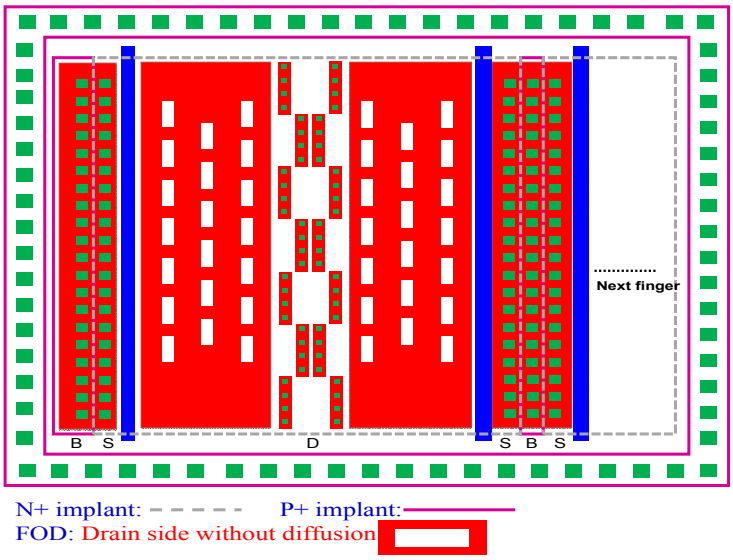

Fig. 3: Schematic layout of an HV nLDMOS with adding FODs and a dotted-OD structure in the drain-side, where the dotted-OD is gap distributed and four contacts involved

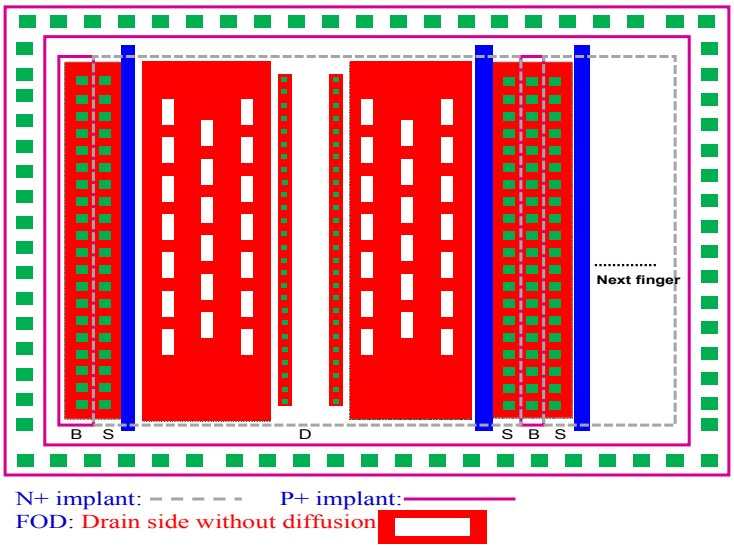

Fig. 4: Schematic layout of an HV nLDMOS with adding FODs and a dotted-OD structure in the drain-side, where the dotted-OD is continuous distributed and 92 contacts involved

edge. On the other hand, the contacts number of a discrete gap dotted-OD region within the central area changed from the minimum one contact (Fig. 2) and gradually increased the contacts number within an OD region to 2, 4 (Fig. 3), 23, 46 and eventually increased to the continuous distributed 92 (Fig. 4). Meanwhile, as the contacts number increased within a dotted-OD region, a dotted-OD layout will be gradually become a stripe-OD type and a non-OD area will distribute in the central zone of drain-side. Moreover, one type of the uniformly distributed dotted-OD layout (Fig. 1) designed to study the influence of contacts distribution on ESD protection robustness, while the dotted-OD has contained only one contact here.

The layout topology we need that is completely symmetric in an nLDMOS device. Both minimum distances should be suited between a contact to a dotted-OD and a drain-side contact to OD on the vertical direction while the channel width is set to be 100-µm. According to the aforementioned description, the maximum number of contacts in a column is 92 and that is the reason why the maximum number of contacts of a continuous distributed OD region is 92. And, in Table 1, the 92 number could be divisible by the contacts in a dotted-OD region, i.e., 1, 2, 4, 23, 46 and 92 contacts, respectively. Therefore, these six kinds of contacts variation will be used in this study. Furthermore, there are two architectures taken as the

Table 1: Experiment parameters of nLDMOS DUTs with adding FODs and dot-OD structures in the drain-side

Sample type	Contacts number	Layout type
I	1	Uniform distributed
II	1	Discrete gap distributed
III	2	Gap distributed
IV	4	Gap distributed
V	23	Gap distributed
VI	46	Gap distributed
VII	92	Continuous distributed

reference DUTs. One is a traditional nLDMOS without adding any FODs and dotted-OD and the other is an nLDMOS only with adding FODs in the drain side.

Testing equipment system: As shown in Fig. 5, a Transmission-Line-Pulse (TLP) system for experimental testing is controlled by the LABVIEW software, which managed the electronic instrument of subsystem such as the ESD pulse generator, the high-frequency digital oscilloscope and the digital power electric meter instruments, in order to achieve the automatic measurement. This machine can provide a continuous step-high square wave to a DUT and shortly raise time of the continuous square wave can also simulate transient noise of an ESD. This HBM-like system has used the short square wave with 100-ns pulse widths and 10 ns rising/falling times to evaluate the voltage and current response of a DUT.

Fig. 5: A TLP testing system

RESULTS AND DISCUSSION

The impacts of an nLDMOS with adding FODs and dotted-OD structures in the drain-side will be tested and discuss as following. Here, as in Table 2, a Ref. traditional nLDMOS DUT (not with any FOD and dotted-OD structures) will be compared with only FOD adding, only dotted-OD adding and dotted-OD varied DUTs to evaluate the influence on ESD immunity. Next, as in Table 1, we will explore the second group of DUTs which changing the number of contacts on dotted-OD structures.

The snapback I-V curves and test results of the group one DUTs (Table 2) are shown in Fig. 6 and Table 2, respectively. As only adding the FODs structure in an nLDMOS device, the resistance of FODs structure is higher but not large enough to cause the I_{t2}

Table 2: Category of nLDMOS DUTs as adding FODs and dotted-OD structures in the drain-side (σ was calculated by 3 DUTs)

FOD_S structure	Dotted-OD structure	Number of contacts in the dotted-OD structure	Layout type of dotted-OD structure	V_{t1} (V)	V_h (V)	I_{t2} (A) (means±σ)
×	×	×	×	88.199	17.539	3.267±0.130
√	×	×	×	85.125	20.511	2.809±0.291
×	√	1	Uniform distribution	89.391	18.676	3.654±0.198
√	√	1	Uniform distribution	89.864	22.068	3.459±0.091
√	√	1	Discrete gap distributed	90.270	21.351	3.180±0.264
×	√	2	Gap distributed	90.053	19.747	3.197±0.232
√	√	2	Gap distributed	90.145	22.615	3.277±0.320

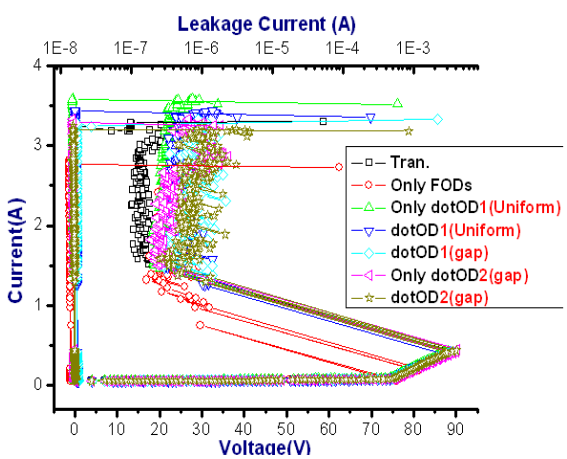

Fig. 6: Snapback I-V curves and leakage currents of HV nLDMOS DUTs as adding FOD and dotted-OD structures in the drain-side

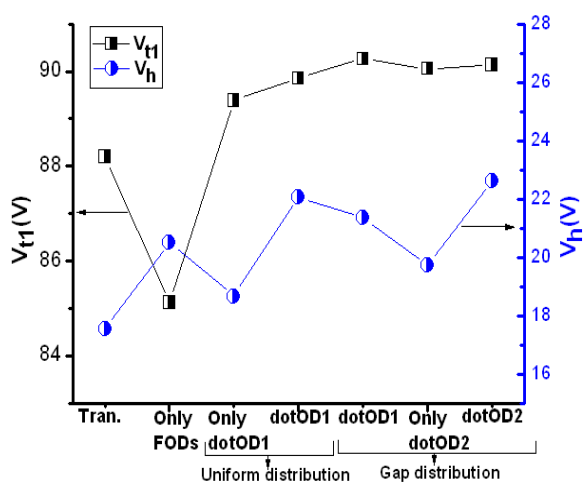

Fig. 7: V_{t1} and V_h distributions by different drain-side engineering

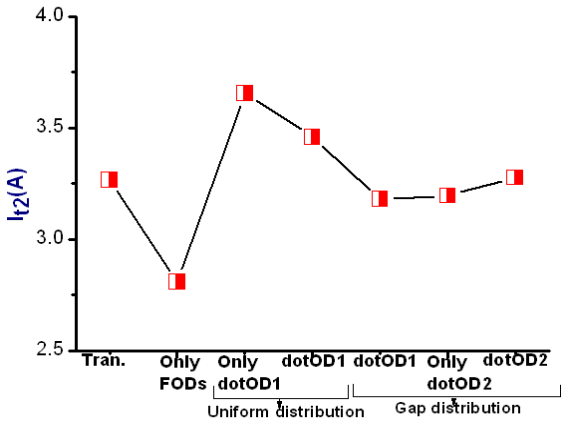

Fig. 8: I_{t2} distributions by different drain-side engineering

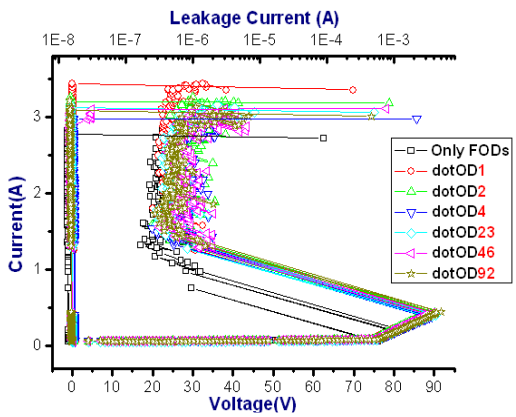

Fig. 9: Snapback I-V curves and leakage currents of HV nLDMOS DUTs as adding only FODs and dotted-OD structures in the drain side

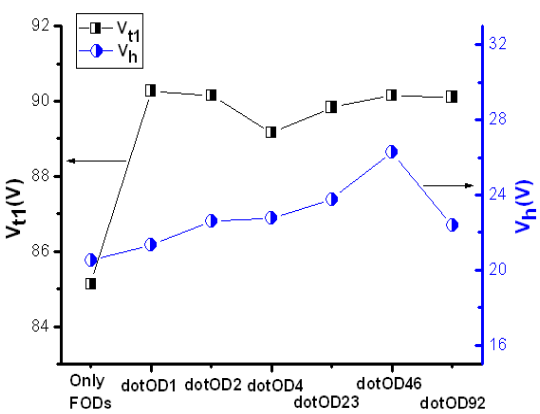

Fig. 10: V_{t1} and V_h distributions by different dotted-OD engineering in the drain side

value of an nLDMOS increased. However, as an nLDMOS device is added the dotted-OD structure, the corresponding I_{t2} value will increase significantly. Then, it shows that a dotted-OD structure is good for ESD current dissipation than an FOD structure, it can make the component with higher ESD current

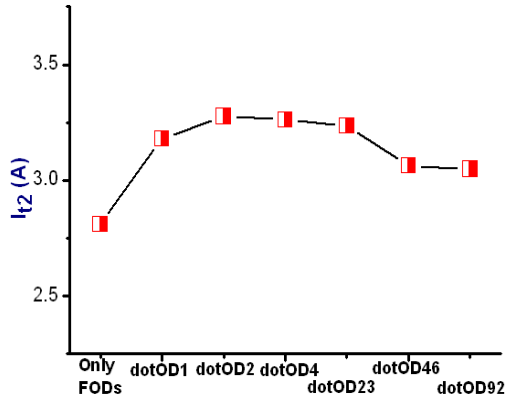

Fig. 11: I_{t2} distributions by different dotted-OD engineering in the drain side

Table 3: Snapback key parameters of dotted-OD engineering in the drain side (σ was calculated by 3 DUTs)

Number of contacts in the dotted-OD structure	V_{t1} (V)	V_h (V)	I_{t2} (A) (mean±σ)
Only FODs	85.125	20.511	2.809±0.291
1 (discrete gap)	90.270	21.351	3.180±0.264
2 (discrete gap)	90.145	22.615	3.277±0.320
4 (discrete gap)	89.156	22.760	3.261±0.629
23 (discrete gap)	89.836	23.788	3.235±0.119
46 (discrete gap)	90.146	26.291	3.064±0.101
92 (continuous)	90.112	22.370	3.049±0.141

capability. The only adding dotted-OD structure not only has higher I_{t2} value but also has higher V_h value than a traditional nLDMOS, so that the dotted-OD structure is worth further developing. However, when a dotted-OD combined with an FOD structure, its I_{t2} value will increase unremarkable, particularly in the discrete gap-distributed types have worse I_{t2} values. The reason for the resistance of FODs adding is higher than a Ref. traditional nLDMOS at high voltage components, so when adding an FOD structure on a dotted-OD area will weaken the ESD capability. The number of contacts on drain-side of a discrete-type layout is less than of a uniform-type layout, which is resulting in a current crowding effect and makes the I_{t2} value of components decreased. However, the most important feature of adding an FOD structure is the V_h value obviously increased, it is good for latch-up immunity in the high voltage environment. And, the layout-type distribution of snapback key parameters of V_{t1}, V_h and I_{t2} are shown in Fig. 7 and 8.

The second group DUTs is contacts number modulation in dotted-OD structures compared with a only FODs adding type. The snapback I-V curves and test results of group two DUTs (Table 3) are shown in Fig. 9 and Table 3, respectively. It can be found that an FOD structure combined with a dotted-OD structure in the drain-side can result in V_h and I_{t2} values increasing. As with more contacts number in a stripe OD, it will have a higher V_h value. When the contacts number of an OD area is 46, it has a maximum value of V_h. The last DUT is a dotOD92 type, which is different layout

architecture (a long stripe OD shown in Fig. 4) of the second group. This layout type makes the drain-side resistance will decrease slightly, which is resulted in the V_h value followed too. In addition, the layout-type distributions of V_{t1} and V_h are shown in Fig. 10. Meanwhile, in the second group DUTs, the distribution aspect of I_{t2} will behave as a bell shape shown in Fig. 11. In dotOD2 and dotOD4 DUTs, they have a best I_{t2} value. Therefore, a proper design of discrete dotted-OD parameter will be good for a component reliability.

CONCLUSION

This study is focused on two crucial subjects, one is the comparison of a Ref. traditional structure, FOD structure and dotted-OD structures in the drain side; the other is an FODs structure combined with a dotted-OD modulated pattern. After systematic tests, it is found that in high-voltage nLDMOS components, adding a FODs structure in the drain side will cause the I_{t2} value of a DUT decreased, but it will be with a higher LU capability. And, dotted-OD structures in the drain side can improve the I_{t2} value of a DUT; meanwhile, the V_h value will not be sacrificed. So that these two structures combined together should be haven a high ESD capability and high LU immunity. Therefore, a combination of these two structures has a high V_h value (25.8% increasing) and the result of I_{t2} compared with a traditional nLDMOS DUT is increased about 5.9%. Nevertheless, experimental results showed that the I_{t2} value of a uniform distributed type is better than a gap-layout type. Therefore, a dotted-OD structure combined with a uniform distributed type should be adopted in the further applications.

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