

Research Article

Design of Optimized Low Power and Area Efficient Digital FIR Filter using Modified Group Structures based Square Root Carry Select Adder

¹S. Murugeswari and ²S. Kaja Mohideen
¹Sri Ramanujar Engineering College,
²B. S. Abdur Rahman University, Chennai, India

Abstract: In Digital Signal Processing, Finite Impulse Response (FIR) filter is mostly used for communications and radar applications. The Performance of FIR filter depends on Multiplier and adder circuits used in filter. To reduce the dynamic power consumption and chip size, different multiplier and adder combinations are used in order to improve the overall performance of FIR filter. The Low Power Modified Square Root Carry Select Adder (M-SQRT CSLA) is presented in this study by introducing half adders instead of full adders. The proposed M-SQRT CSLA has been designed to reduce dynamic power consumption. Hence the modified SQRT CSLA is applied into Wallace multiplier for addition process after the partial product generation stage. MAC unit of the Digital FIR filter is designed by using modified Wallace multipliers and M-SQRT CSLA. Further the Group 2, Group 3; Group 4 and Group5 structures of SQRT CSLA were constructed using half adders only. Comparison between proposed SQRT CSLA and Modified Carry Save Adder (MCSA) has been done with reference to the Area, Power and Delay. It is proved that the proposed SQRT CSLA consumes less area and power than all other methods. Simulation is performed by Modelsim6.3c and Synthesis process is done by Xilinx 10.1. The simulation result shows that digital filter with proposed SQRT CSLA occupies less area and consumes low power.

Keywords: Digital FIR filter, DSP, MAC unit, MCSA, Modified SQRT CSLA

INTRODUCTION

The optimization of Area, Power and delay in digital circuits is very much essential. In Ripple Carry Adder, the sum for each bit position in basic adder is produced sequentially only after the previous bit position has been summed and a carry propagates into the next position. The regular CSLA consists of two sets of Ripple carry adders for $c_{in} = 0$ and $c_{in} = 1$. The CSLA is used in several systems to reduce the carry propagation delay by independently generate the multiple carries and then choose a carry to generate the sum (Kim and Kim, 2001).

The SQRT CSLA is used for various multiplier circuits in order to reduce the carry propagation delay. There are various combinations of CSLA are available for achieving low delay and occupancy of low area. In two sets of RCAs, One RCA can be replaced by either D-Latch or Binary to Excess1 code Conversion (BEC) for providing efficient low computation and low area. In Our Proposed work, the SQRT CSLA is done by half adders instead of full adders used in conventional SQRT CSLA. Therefore, the area occupancy is reduced for providing partial sum and carry in addition process. This Modified SQRT CSLA (M-SQRT CSLA) is

further applied to Wallace tree multiplier in order to achieve optimization of low power and area efficiency. For Digital Signal Processing FIR filters is one of the important tools for mobile and radar application. But In FIR, Multiplication and addition gives the more complexity and lower performance. Therefore in our work, Wallace tree multiplier with M-SQRT CSLA used to design the FIR filter for achieving high performance. Further comparisons of conventional SQRT CSLA and Modified-SQRT CSLA are presented in this study. Result shows that the Modified Carry Select Adder minimizes area and delay and it offers lesser power than any other combinations with CSLA.

LITERATURE SURVEY

The delay is caused by carry propagation is one of the major impacts while analyzing the digital adder circuit. To reduce the carry propagation delay, carry select adder (CSLA) is used here. Carry look-ahead adder consumes more area for computing than CSLA. 16-bit, 32-bit, 64-bit additions were performed with low delay and low power by using conventional CSLA. The conventional carry select adder having Dual RCAs was proposed in He *et al.* (2005). This CSLA provide

efficient compromise between RCA and carry look-ahead adder. The partial sum and carry are generated by this efficient CSLA while considering input carry as '0' and '1' and therefore, final sum and carry are selected by multiplexers. In Shanigarapu and Shrivastava (2013), the effective CSLA was proposed by using one RCA and D-Latch for providing partial sum and carry. D-Latch consumes Low delay when compared to regular CSLA with Dual RCAs. In Saxena *et al.* (2013), D-latch in CSLA is replaced by Binary to Excess1 code Conversion (BEC) to provide partial sum and carry consumes less area, power and delay. This provides less delay for 128-bit addition. This architecture is mostly used for FIR filter in order to reduce dynamic power consumption and meet the computational efficiency. The performance of above computational was done by Ripple Carry Adder, Carry Look ahead adder, CSLA with various combinations such as Dual RCAs, One RCA and One D-Latch, One RCA and One BEC unit are analyzed and compared in Mohanty and Patel (2014). The CSLA with One RCA and One BEC consumes lower area and delay when compared to other CSLA structures (Mohanty and Patel, 2014). In Our Proposed work, we design modified CSLA with Half Adders and Multiplexers only. Half Adder consumes less area when compared to full adder and therefore this study is used to make low power and efficient area FIR filter design.

Modified carry save adder: Conventional Carry Save Adder structure yields large carry propagation delay. To minimize the time consumption, a MCSA was proposed by Ramkumar *et al.* (2010). In the Modified Carry Save Adder, the final stage of CSA is divided into 5 groups. The first group incorporates $n(1+\log_2 n)$ -bit value and additional groups include $\log_2 n$ -bit value, where n is indicating the bit size of the adder. The separated groups are listed as follows:

- $\{c4, s [4:0]\}$, output $s [4:0]$ is straightforwardly allocated as the final output.

- $\{c7, x [7:5]\}$ manages the partial result by considering $c4$ is 0.
- $\{c10, x [10:8]\}$ exercise the fractional result by taking into consideration as $c7$ is 0.
- $\{c13, x [13:11]\}$ manipulates the limited result by making an allowance for $c10$ is 0.
- $\{X [17:14]\}$ manipulates the partial result keeping $c13$ is 0.

The most important benefit of this logic is that each set work outs the partial results in concurrent manner and the multiplexers are prepared to provide the final result instantly with the lowest delay. If the C_{in} of each group arrives, the final result will be determined immediately. Thus the maximum delay is reduced in the carry propagation path. The area gives the total cell area and the total power is the summation of internal power, net power, leakage power and dynamic power. Result shows that the Modified Carry Save Adder (MCSA) has minimized area and delay and offers lesser power than CSA (Parhi, 1998).

Conventional Sqrt CSLA: Compared with MCSA, further to reduce the area and power, an attempt was made by Wey *et al.* (2012) and they proposed a square root CSLA with BEC (Binary to Excess1 code Converter). The conventional Sqrt CSLA consists of Ripple carry adder and BEC as shown in Fig. 1 whereas RCA or D Latch were used in earlier architectures (He *et al.*, 2005).

The Conventional Group 2, Group 3 and Group 4 structures are shown in Fig. 2 which contain full adder, half adder, Binary to Excess1 code Converter and multiplexer units. Conventional Sqrt CSLA offers lower delay and high speed than the previous architectures (Ramkumar and Kittur, 2012). Further to reduce the area, power and delay, a new Sqrt CSLA architecture has been designed and analyzed in next section.

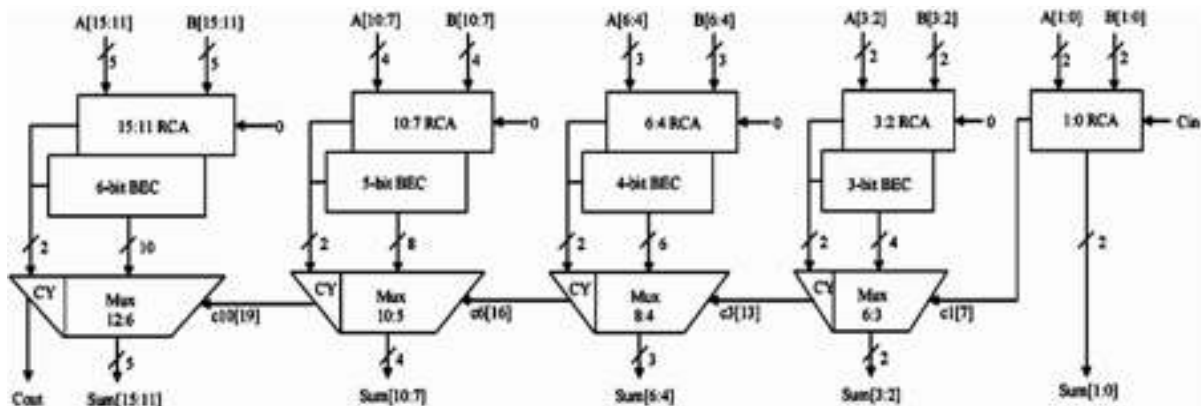


Fig. 1: Block diagram of conventional Sqrt CSLA using BEC structure

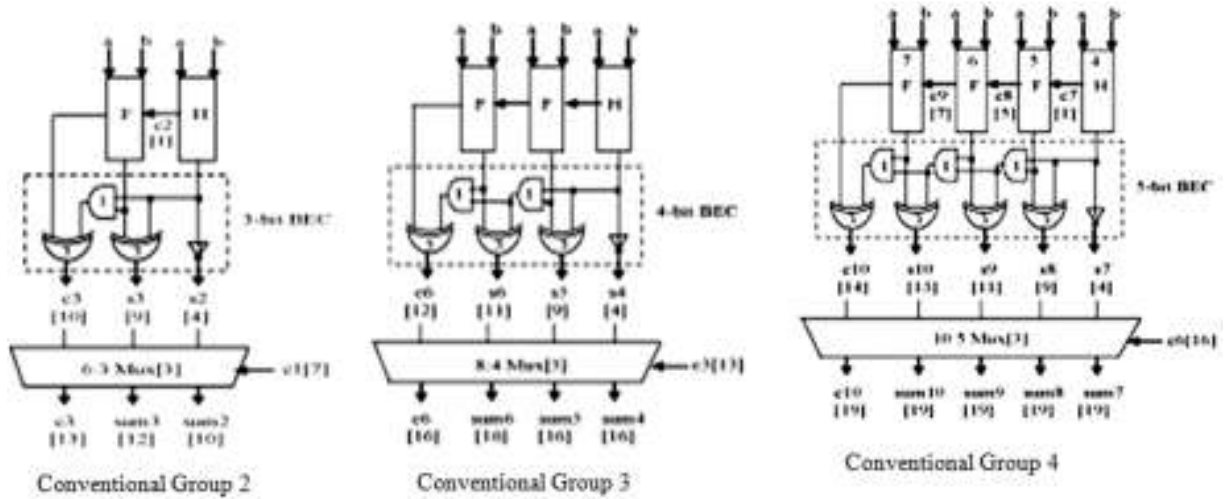


Fig. 2: Block diagram of conventional Group 2, Group 3 and Group 4 structures

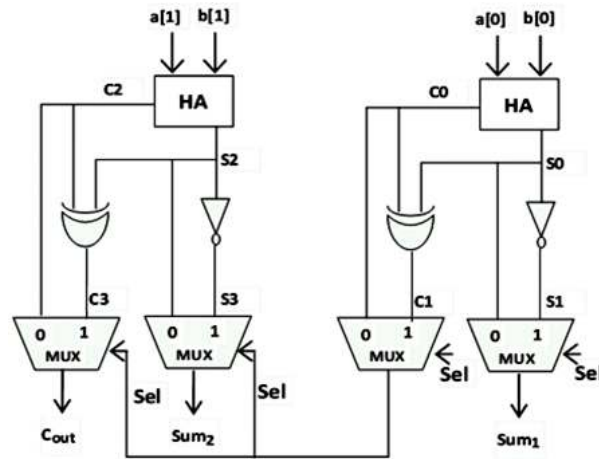


Fig. 3: Circuit diagram of modified Group 2 structure for proposed SQR CSLA

In this study, design and analysis of Modified SQR Carry Select Adder has been carried out, (Pravin and Palaniappan, 2013). This adder is incorporated in the Wallace Multiplier which is then used in the design of digital FIR filter. The propagation delay of Carry Save Adder is increased due to carry propagation. Hence Carry Select Adder is redesigned to reduce the delay, area and power. Further to reduce the area and power, regular SQR CSLA is modified by introducing half adders, inverter and 2:1 multiplexer (Shuchi and Sampath, 2014).

Proposed SQR CSLA: In this study, the group 2 architecture of conventional SQR CSLA is modified to have two Half adders, one XOR gate, one Inverter and two 2:1 multiplexers as shown in Fig. 3. Hence proposed group 2 structure has twelve gates and four 2:1 multiplexer only where as the existing group 2 structure has 18 gates and one 2:1 mux. Similarly

Group 3, Group 4 and Group 5 are designed by introducing half adders, inverter, XOR gate and 2:1 MUX only. All these Group Structures (Fig. 3 to 5) are used to design a 16-bit SQR CSLA architecture as shown in Fig. 6.

The proposed SQR CSLA has been simulated and the simulation results are compared with various existing CSLA architectures namely Regular SQR CSLA using RCA, BEC and D Latch and the results are shown in the Table 1.

The performance comparison of proposed SQR CSLA with other SQR CSLAs is shown in Fig. 7. It can be seen that the proposed SQR CSLA consumes low power and has lesser area when compared to other SQR CSLAs.

Modified wallace multiplier using proposed SQR CSLA adder: Since adder is a vital part of all multiplier blocks, the modified SQR CSLA is

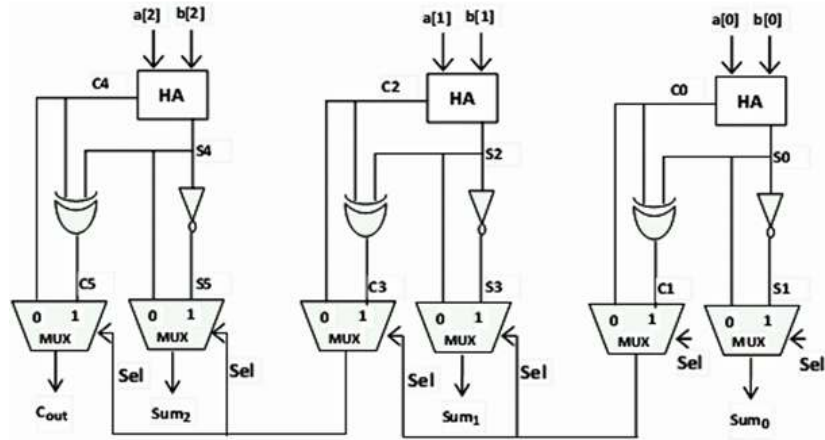


Fig. 4: Circuit diagram of modified Group 3 structure for proposed Sqrt CSLA

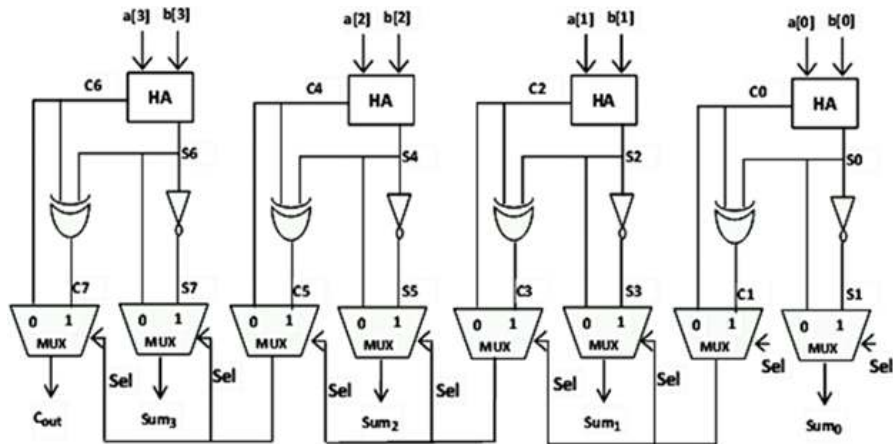


Fig. 5: Circuit diagram of modified Group 4 structure for proposed Sqrt CSLA

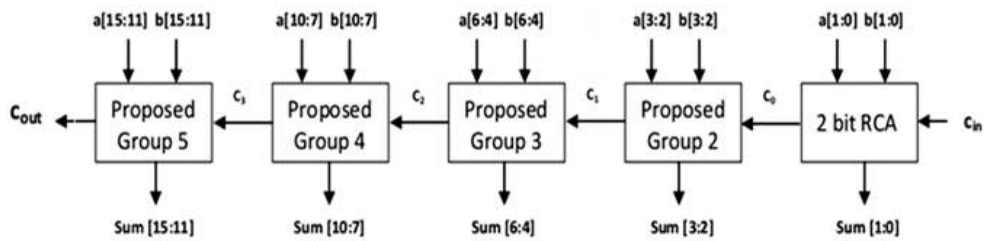


Fig. 6: Block diagram of proposed 16-bit Sqrt CSLA

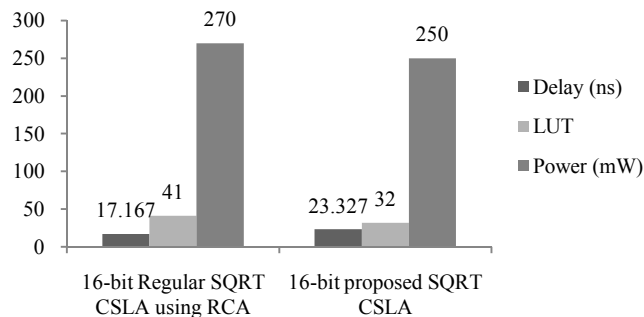


Fig. 7: Performance comparison of proposed Sqrt CSLA with regular Sqrt CSLA

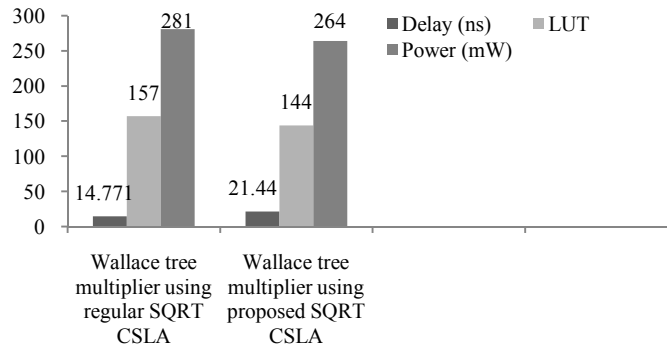


Fig. 8: Performance comparison of Wallace multiplier using proposed Sqrt CSLA and regular Sqrt CSLA

Table 1: Comparison of proposed Sqrt CSLA with regular Sqrt CSLA

Different types of adder	LUT	Delay (ns)	Power (mW)
16-bit regular Sqrt CSLA using RCA	41	17.167	270
16-bit proposed Sqrt CSLA	32	23.327	250

Table 2: Comparison of Wallace multiplier with proposed Sqrt CSLA and regular Sqrt CSLA

Method	Delay (ns)	LUT	Power (mw)
Wallace tree multiplier using regular Sqrt CSLA	14.771	157	281
Wallace tree multiplier using proposed Sqrt CSLA	21.440	144	264

incorporated in the Wallace Multiplier in order to have reduction in delay, area and power. The modified Wallace multiplier has reduced amount of half adders when compared to the conventional Wallace multiplier (Waters and Swartzlander, 2010). In the modified circuit, N^2 AND gates form the partial products and they are set in an inverted triangle order. The matrix is divided into three row groups in the modified Wallace reduction method (Rajaram and Vanithamani, 2011):

- Full adder is used for adding three bits
- Single bit and a group of two bits are moved to the next stage directly

Simulation of Wallace multiplier with Modified Carry Save Adder, regular Square Root Carry Select Adder (Sqrt CSLA) and Modified Square Root Carry Select adder has been made and implemented in Spartan 3 XC3S50 (package: pQ208, speed grade: -5) FPGA using the Xilinx ISE 10.1i design tool.

Total equivalent LUT in case of Wallace multiplier using Regular Sqrt CSLA is 157 where as it is reduced to 144 using proposed Sqrt CSLA based Wallace multiplier. The power consumption in case of Wallace multiplier using Regular Sqrt CSLA is 281 mW, which is reduced to 264 mW using proposed Sqrt CSLA based Wallace multiplier. The comparison results are tabulated as shown in Table.2. Fig. 8 shows the Performance comparison of Wallace multiplier using proposed Sqrt CSLA and regular Sqrt CSLA in terms of delay, LUT and power.

On comparing the above circuits in terms of power consumption, it can be seen that the Wallace multiplier using proposed Sqrt CSLA consumes much less

power (264 mW) which is 6 % less than Wallace multiplier using Regular Sqrt CSLA.

DIRECT FORM FIR FILTER USING MODIFIED WALLACE MULTIPLIER AND Sqrt CSLA

The modified Wallace Multiplier has been incorporated in Digital FIR filter which requires MAC (Multiplication and Accumulation) Unit to perform coefficient multiplication and addition (Parhami, 2010). The FIR filter using the modified Wallace Multiplier with proposed Sqrt CSLA has better area reduction and low power consumption.

The structure of Direct Form FIR filter is shown in Fig. 9 which consists of adders, multipliers and delay units. In the fixed point calculation of FIR (Finite Impulse Response) filter, full operand bit-width of the multiplier outputs is commonly used i.e., When the bit-widths of coefficients and data inputs are 8, the multiplier produces 16-bit output. Similarly all other taps are processed and added using 16-bit adder.

In this study, a 3-tap Direct Form FIR filter has been designed using modified Wallace Multiplier and Square Root Carry Select Adder.

The proposed FIR filter is compared with the conventional FIR filter using regular Wallace multiplier and Square Root Carry Select Adder. From the comparison, it can be seen that the proposed FIR filter consumes less area and power than conventional FIR filter. FIR comparison results are tabulated in Table 3. Figure 10 shows the performance comparison of proposed FIR filter over conventional FIR filter.

Table 3: Comparison of FIR filters using modified Wallace multiplier with regular CSLA and proposed CSLA

Method	Delay (ns)	LUT	Power (mw)
FIR filter using Wallace tree multiplier with regular Sqrt CSLA	10.825	68	270
FIR filter using Wallace tree multiplier with proposed Sqrt CSLA	10.881	66	251

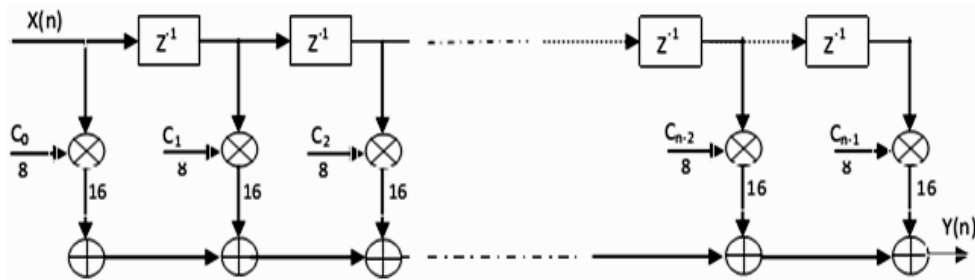


Fig. 9: Block diagram of direct form FIR filter

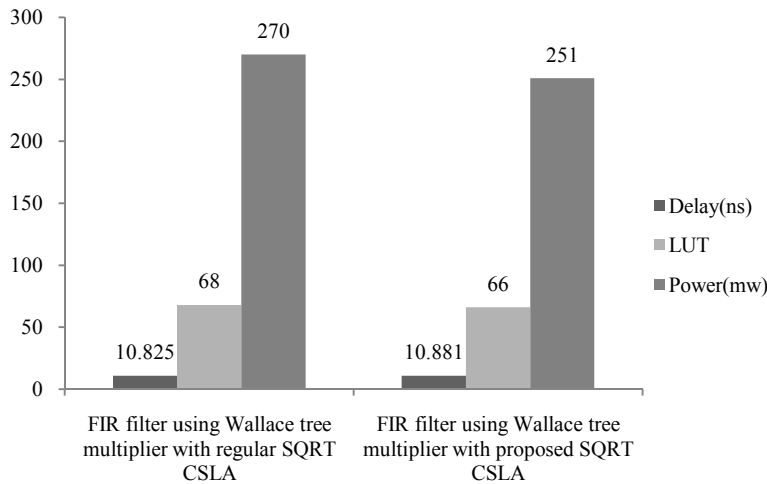


Fig. 10: Performance comparison of FIR filters using Wallace multiplier with regular CSLA and proposed CSLA

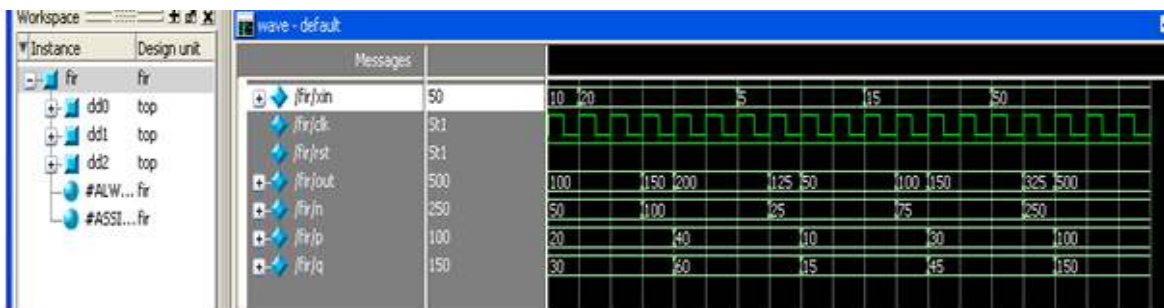


Fig. 11: Simulation results of proposed FIR filter using Modified Sqrt CSLA and Wallace multiplier

Fir filter simulation output: The Fig. 11 illustrates the simulation results of FIR filter using Wallace tree multiplier with proposed Sqrt CSLA. Simulation of Wallace multiplier with Modified Carry Save Adder, regular Square Root Carry Select Adder (Sqrt CSLA) and Modified Square Root Carry Select adder has been made and implemented in Spartan 3 XC3S50 (package: pQ208, speed grade: -5) FPGA using the Xilinx ISE 10.1i design tool.

CONCLUSION

In this study, an area efficient and low power proposed Sqrt CSLA is designed. This adder has been incorporated in the reduced complexity Wallace multiplier and then this multiplier structure has been used to design a 3-tap Direct Form FIR filter. This proposed FIR filter is compared with the regular FIR filter. The simulation result shows that the proposed

FIR filter occupies lesser area and consumes lower power than the regular FIR filter. The simulation result shows that the proposed FIR filter occupies lesser area and consumes lower power than the conventional FIR filter.

REFERENCES

- He, Y., C.H. Chang and J. Gu, 2005. An area-efficient 64-bit square root carry-select adder for low power application. *Proceeding of IEEE International Symposium on Circuits System*, 4: 4082-4085.
- Kim, Y. and L.S. Kim, 2001. 64-bit carry-select adder with reduced area. *Electron. Lett.*, 37(10): 614-615.
- Mohanty, B.K. and S.K. Patel, 2014. Area-delay-power efficient carry-select adder. *IEEE T. Circuits-II*, 61(6): 418-422.
- Parhami, B., 2010. *Computer Arithmetic: Algorithms and Hardware Designs*. 2nd Edn. Oxford University Press, New York, NY.
- Parhi, K.K., 1998. *VLSI Digital Signal Processing*. Wiley, New York, NY, USA.
- Pravin, J. and C. Palaniappan, 2013. An area and delay efficient CSLA architecture. *IOSR J. Electron. Commun. Eng. (IOSR-JECE)*, 5(3): 20-25.
- Rajaram, S. and K. Vanithamani, 2011. Improvement of Wallace multipliers using parallel prefix adders. *Proceeding of International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN, 2011)*, pp: 781-784.
- Ramkumar, B., H.M. Kittur and P.M. Kannan, 2010. ASIC implementation of modified faster carry save adder. *Eur. J. Sci. Res.*, 42(1): 53-58.
- Ramkumar, B. and H.M. Kittur, 2012. Low-power and area-efficient carry-select adder. *IEEE T. VLSI Syst.*, 20(2): 371-375.
- Saxena, P., U. Purohit and P. Joshi, 2013. Analysis of low power, area-efficient and high speed fast adder. *Int. J. Adv. Res. Comput. Commun. Eng.*, 2(9).
- Shanigarapu, L. and B.P. Shrivastava, 2013. Low-power and high speed carry select adder. *Int. J. Sci. Res. Publ.*, 3(8).
- Shuchi, V. and K.V. Sampath, 2014. Design and analysis of low power, area-efficient carry select adder. *Int. J. Eng. Res. Appl.*, 4(3): 53-55.
- Waters, R.S. and E.E. Swartzlander, 2010. A Reduced Complexity Wallace multiplier reduction. *IEEE T. Comput.*, 59(8): 1134-1137.
- Wey, I.C., C.C. Ho, Y.S. Lin and C.C. Peng, 2012. An area-efficient carry select adder design by sharing the common Boolean logic term. *Proceeding of the International MultiConference of Engineers and Computer Scientists (IMECS, 2012)*, pp: 1-4.