Research Journal of Applied Sciences, Engineering and Technology 9(2): 138-144, 2015
DOI:10.19026/rjaset.9.1388
ISSN: 2040-7459; e-ISSN: 2040-7467
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Submitted: October 15, 2014 Accepted: November 13, 2014 Published: January 15, 2015

Research Article

3D ICs-power Analysis Using Cylindrical and Co-axial Through Silicon Via (TSV)

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Abstract: In this study, analytical model and electrical equivalent circuit of Through Silicon Via (TSV) is analyzed. Through silicon Vias form an integral component of the 3-D IC technology by enabling vertical interconnections in 3-D ICs. Among various types, the performances of the simplified lumped TSV model of cylindrical and co-axial type were studied. The performance analyses of these structures were presented by introducing these structures between the tiers of digital circuits. The power consumption of the transistor level digital circuits for single tier without TSV and multiple tiers with cylindrical TSV and Co-axial TSV was simulated using Virtuoso Schematic Editor of Cadence. The comparison for cylindrical and co-axial TSV model with different level tiers were tabulated and performed.

Keywords: Three-dimensional ICs, Through Silicon Via (TSV), TSV lumped RLC model

INTRODUCTION

To increase the functionality and Integration density, the recent advancements in semiconductor processing technologies have enabled three dimensional circuit designs and implementation of heterogeneous systems in the same platform, i.e., Flash, DRAM and SRAM placed on top of logic devices and microprocessor cores (Knickerbocker *et al*., 2008). 3-D Integration has been considered as the leading technology to overcome the planar IC scaling down limitations such as increased power consumption, wire delay, process variation and cost with the technical node evolution. 3D IC technology helps in mitigating the interconnect problems by reducing the global interconnect wiring length and simultaneously reducing the chip area. Many long interconnects required in 2D chips can be replaced by a 3-D chip by short vertical interconnects. This improves the circuit performance and reduces the total wiring length needs for a system (Van Olmen *et al*., 2008). Among, Several 3-D integration technologies that have been explored recently, 3D TSV (Through Silicon via) Architecture has proven to be the key enabling Technology.

Through Silicon Via (TSV) is a vertical interconnect element which connects multiple dies and routes the electrical signal and power supply path through all the chips in the stack. TSVs shorten the chip-to-chip interconnects, enable products with higher electrical performance, lower power consumption, wider bandwidth, higher density, smaller form factor, lighter weight and eventually lower cost (Xu and Lu, 2012). The Main applications of TSV are of WLAN, cellular applications and for high performance server and super computer chips. Today there is a variety of TSV structures fabricated and characterized, with various sizes, heights, aspect ratios, materials, densities and processes such as cylindrical TSV, tapered TSV, annular TSV, co-axial TSV, etc. Depending on its structural merits, coaxial through-silicon via (TSV) which has explored recently is a promising 3-D integration solution, which can offer lower coupling with its surrounding environment and achieve better electromagnetic compatibility and signal integrity than other TSV structures (Xu and Lu, 2012). The objective of this study is to analyze the parameters of TSV Model and the performance comparison of Cylindrical and Co-axial TSV RLC Model by introducing these structures between the tiers are verified by using the Virtuoso Schematic Editor. Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics.

MATERIALS AND METHODS

In the 3-D TSV first approach (Van Olmen *et al*., 2008), TSVs are fabricated after FEOL processing and before BEOL processing and enable the interconnection between the Top Metal of the bottom tier and Metal1 of the top tier is as shown in the cross section of Fig. 1. Electrodynamic principles aid in understanding the impact of physical and technological parameters on R_{TSV}, L_{TSV} and C_{TSV}.

Cylindrical model: It is the most common TSV scheme where a cylindrical or square conductive metal

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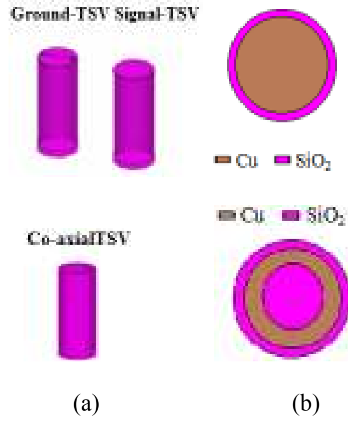


Fig. 1: (a) Three dimensional view and (b) Top view of TSV

layer is surrounded by an isolation layer. Due to a thin isolation dielectric (ILD) layer and large extension through Si, electrical parasitic coupling and critical substrate noise can occur in neighboring active devices and between two TSVs. Signal transmission in TSVs impacts neighboring transistor body voltage such that circuit performance in both digital and analog applications are significantly impacted despite placing substrate ties to ground next to TSVs (Rousseau *et al*., 2008; Khan *et al*., 2009). The equivalent electrical model of ground-signal TSV configuration with analytic RLCG parameters are shown in Fig. 2a as referred from Liang *et al*. (2013) and the Closed-form equations of the analytical RLC electrical model of TSV shown in Fig. 2b were derived and validated.

R_{TSV} model: The values of the parasitics are derived as a function of physical parameters, material characteristics and technology parameters. The analytical expression of the dc resistance of the TSV with respect to its radius is given by:

$$R_{TSV_DC} = \frac{\rho l_{TSV}}{\pi r_{TSV}^2} \tag{1}$$

For high-frequency signals, however, the increase in resistance due to skin effect should be accounted. Expressions derived by Goldfarb and Pucel (1991) are used to derive the R_{TSV_AC} for higher frequencies. With Cu as TSV conductor, the resistivity is 16.8 nΩ m and where skin effect is quite significant for higher diameter TSV structures.

L_{TSV} model: The partial self-inductance of the TSV depends upon the diameter and length of the TSV and is given by the following empirical expression:

$$L_{TSV_SELF} = \frac{\mu_0}{4\pi} \left[2l_{TSV} \ln\left(\frac{2l_{TSV} + \sqrt{r_{TSV}^2 + (2l_{TSV})^2}}{r_{TSV}} \right) + \left(r_{TSV} - \sqrt{r_{TSV}^2 + (2l_{TSV})^2} \right) \right] \tag{2}$$

where, μ_0 is the permeability of free space given by H/m. Additionally, mutual inductance between TSVs has an impact on the overall inductance parasitic of a TSV. Depending on the location and spacing between the neighboring TSVs, mutual inductance can have an additive effect when the current flow is in the same direction and a diminutive effect when current flows on opposite direction, i.e., between a power and ground TSV. Mutual inductance between two TSVs can be derived as:

$$L_{MUTUAL} = \frac{\mu_0 l_{TSV}}{2\pi} \cdot \left[\ln\left(\frac{l_{TSV}}{s_{TSV}} + \sqrt{1 + \left(\frac{l_{TSV}}{s_{TSV}}\right)^2} \right) - \sqrt{1 + \left(\frac{s_{TSV}}{l_{TSV}}\right)^2} + \frac{s_{TSV}}{l_{TSV}} \right] \tag{3}$$

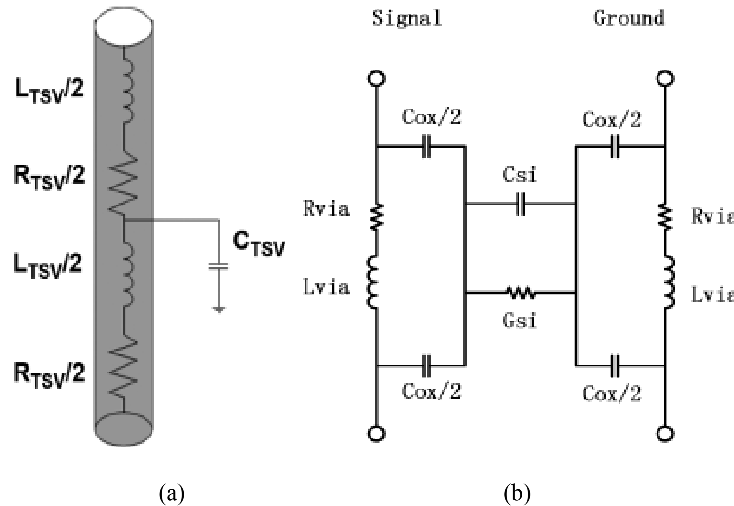


Fig. 2: (a): Electrical model of a TSV; (b): equivalent circuit of cylindrical TSV

where, s_{TSV} is the spacing between two TSVs. Spacing between two TSVs varies depending on their location. For example, the mutual coupling between two neighbor TSVs in either vertical or horizontal direction have a space m, while two TSVs mutually coupled in diagonal direction have a space m:

$$L_i^{VDD} = L_{self_i}^{VDD} + \sum_{j \varepsilon neighbors} \alpha_j L_{M_j}^{VDD} - \sum_{k \varepsilon neighbors} \alpha_k L_{M_K}^{GND} \quad (4)$$

$$L_i^{GND} = L_{self_i}^{GND} + \sum_{j \varepsilon neighbors} \alpha_j L_{M_j}^{GND} - \sum_{k \varepsilon neighbors} \alpha_k L_{M_K}^{VDD} \quad (5)$$

where, L_i^{VDD} is the inductance for a power TSV and L_i^{GND} is the inductance for ground TSV. Coefficient is the ratio of currents flowing through the TSV under investigation and its neighboring TSV as the current flow on each TSV can differ based on the switching activity of the underlying circuits. For example, a TSV located on the boundary of the TSV array has fewer neighboring TSVs than a TSV located in the center of the TSV array. Hence their mutual inductance would vary. Additionally, mutual inductance varies with respect to the distance between TSVs, as the space between two TSV increases, their coupling decreases as well.

C_{TSV} model: TSV capacitance can be derived by solving Poisson's equations for MOS capacitor structure in cylindrical coordinate system due to TSV shape (Topol *et al*., 2006).

It is sufficient to solve 1-D Poisson's equation along radial direction to obtain the capacitance (Katti *et al*., 2010). Equation (6) describes TSV capacitance as a function of oxide and depletion capacitance as:

$$C_{TSV} = \frac{C_{OX}\, C_{dep_{\min}}}{C_{OX} + C_{dep_{\min}}} \quad (6)$$

where,

$$C_{OX} = \frac{2\pi\varepsilon_{OX}\, l_{TSV}}{\ln\left(\frac{R_{OX}}{R_{metal}}\right)},\ C_{dep_{\min}} = \frac{2\pi\varepsilon_{si}\, l_{TSV}}{\ln\left(\frac{R_{\max}}{R_{OX}}\right)}$$

where, $\varepsilon_{OX}, \varepsilon_{si}$ are permittivity of oxide and silicon, respectively. As shown in (4), C_{TSV} is directly proportional to the length of TSV and inversely proportional to the dielectric thickness of TSV. With increasing frequency up to 20 GHz, for different μm diameter TSV, its capacitance drops off from 30 to 5 fF (Bermond *et al*., 2009). In this study, we utilize parasitic values obtained for different TSV geometries are listed in Table 1.

Co-axial model: Coaxial TSVs, first proposed by Sparks *et al*. (2006) can eliminate substrate noise by grounding the outer metal layer while the inner metal layer is used for signal transmission. This makes coaxial TSVs self-shielded and isolated from their surrounding environments. The space between the inner and outer conductors (usually made from copper) can be filled with a low-loss isolation dielectric, e.g., benzocyclobutene (BCB), or silicon substrate.

Electrical characteristics of coaxial TSVs are usually studied with an equivalent circuit model, i.e., a lossy transmission line model and the RLC parameters of coaxial TSVs can be calculated by using the following simple closed-form formulas.

R_{TSV} model: The analytical expression of the series resistance of the TSV with respect to its radius and per unit length is given by:

$$R_{TSV} = \frac{1}{2\pi\delta\sigma}\left(\frac{1}{a} + \frac{1}{b}\right) \quad (7)$$

where, δ is the skin depth, σ is the TSV conductivity are inversely proportional to the resistance of the TSV. a and b are radius of inner and the outer surface of the conductor.

L_{TSV} model: The series conductance per unit length is given by:

$$L_{TSV} = \frac{\mu_0\mu_r}{2\pi}\ln\left(\frac{b}{a}\right) \quad (8)$$

C_{TSV} model: The TSV capacitance is the series combination of the oxide and depletion capacitance. The capacitance per unit length is given by:

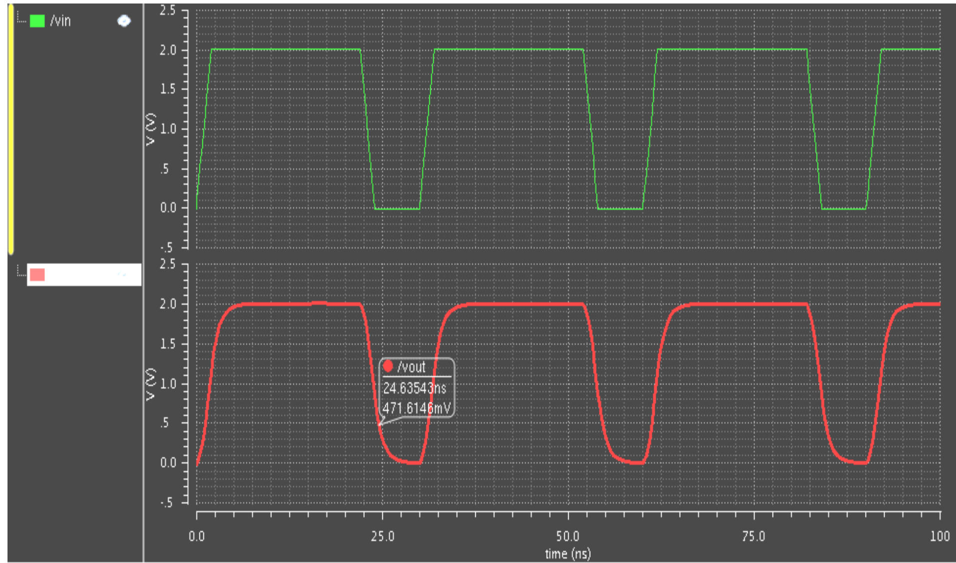
$$C_{TSV} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{b}{a}\right)} \quad (9)$$

RESULTS AND DISCUSSION

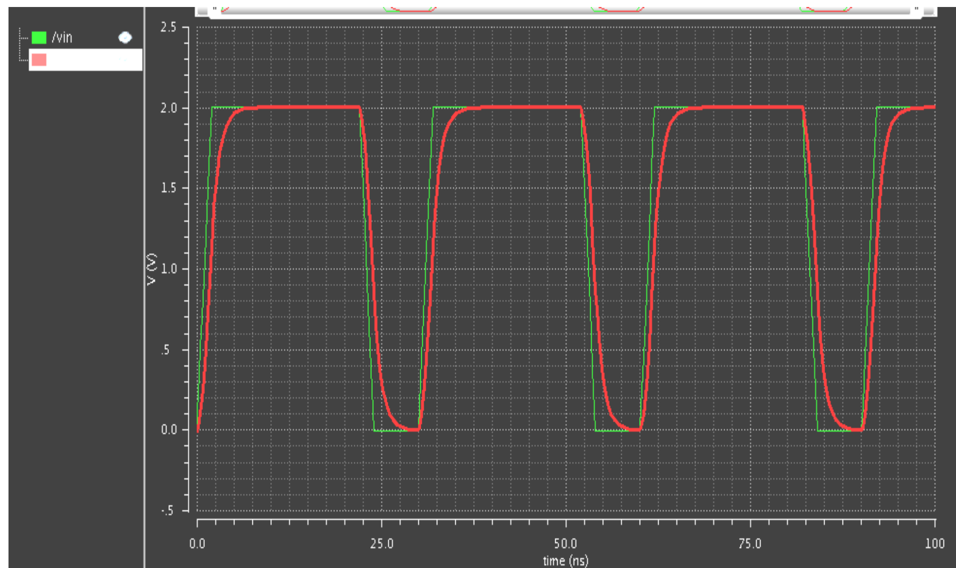
In the Lumped *RLC* model of a TSV, the *R*TSV and *L*TSV cause the voltage drop along the interconnected

Table 1: Parasitic values of a TSV

TSV Diameter (μm)	TSV Oxide Thickness (nm)	TSV Length (μm)	$R_{TSV\ DC}$ (mΩ)	L_{TSV} (pH)	C_{TSV} (fF)
2	50	20	118.49	13.827	52.229
2	100	20	132.02	14.039	21.429
5	50	50	44.539	34.262	69.982
5	100	50	46.414	34.521	35.889



(a)



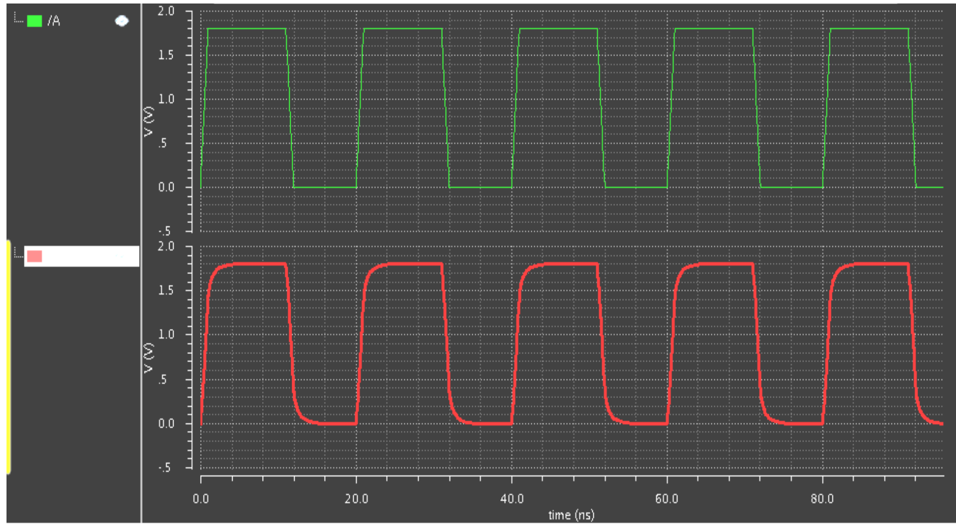
(b)

Fig. 3: The above figure shows the transient response of RC delay model between two tiers

nodes between Metal1 of the top tier and Top Metal of the bottom tier. *C*TSV is connected between TSV and ground. *L*TSV is predominant only for clock frequencies with rise and fall times above 3 GHz. As referred from Katti *et al*. (2010), the approximate model is obtained by ignoring the inductance which reduces to a simplified *RC* model. The impact of RTSV and CTSV on the TSV delay can be analyzed with the help of placing the circuit between the inverters. The circuit consists of an inverter placed on the bottom tier driving an inverter on the top tier through TSV RC model. RTSV would cause a minimal impact on the delay.

A predominant impact of CTSV and a reduced impact of RTSV is analyzed, with inverters in alternate tiers connected by TSVs is simulated using Spectre Simulator. RTSV and CTSV are varied and their impact on delay is verified. The RC model and the RLC model of cylindrical and co-axial TSV between the tiers were designed using Virtuoso Schematic tool and its simulated results are shown below.

The input signal Vin (where tr = tf = 2ns, T = 30 ns) given at one end of the RLC model and the output taken Vout at other end without placing them in between tiers is shown in Fig. 3a. By changing the values of CTSV in RC model, the increase in delay and the voltage drop occurs in its output, than the effect of varying the RTSV is shown in Fig. 3b.



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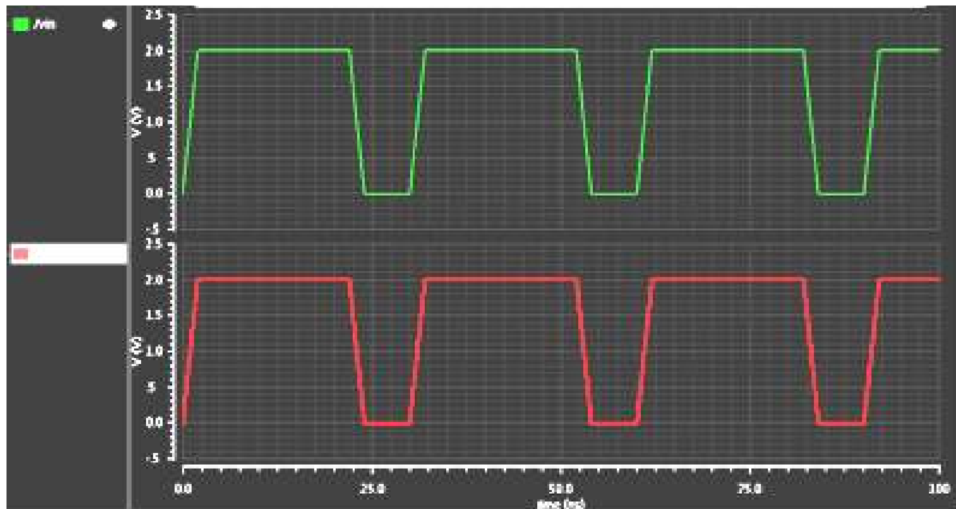

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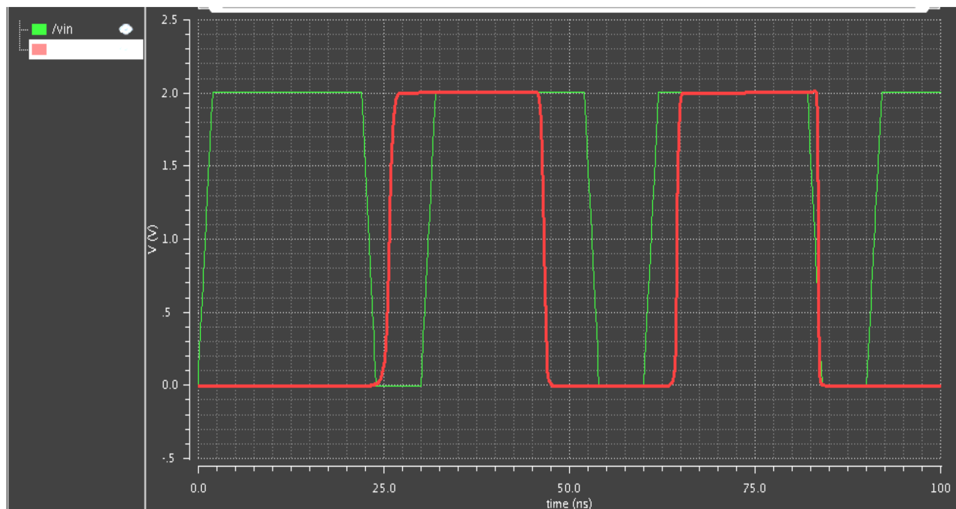
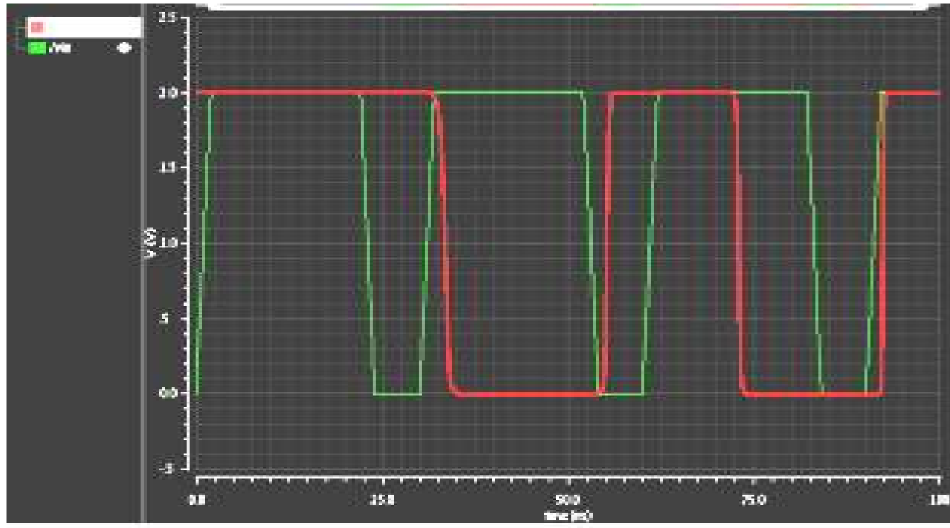


(c)



(d)

Fig. 4: The above figure (a) and (b) shows the transient response of cylindrical and Co- axial TSV RLC model and (c) and (d) shows the response of placing them between two tiers

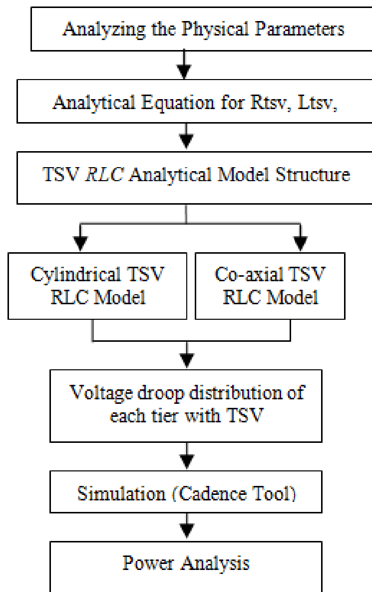


Fig. 5: Power analysis flow model

Next, the transient response for both the Cylindrical and Co-axial TSV RLC model between tier levels is also analyzed to determine the impact on delay of the TSV RLC Model in 3D Integration is as shown below in Fig. 4. In the analysis, the variations in RTSV values for a given value of CTSV do not change the delay significantly but delay increases significantly with increasing CTSV. Thus, changes in RTSV show minimal impact on the delay, while the impact of CTSV is not negligible. When the number of tier level increases the delay and the voltage drop increases significantly and can be minimized by changing the parameter values of CTSV.

Table 2: Comparison table for power analysis of TSVs

Number No. of tiers	Without TSV model (mW)	With cylindrical TSV(mW)	With Co-axial TSV(mW)
2 TIER	0.1310	0.525	0.4078
3 TIER	0.1358	1.568	1.4257
4 TIER	0.1408	1.861	1.6734
5 TIER	0.1462	2.153	1.968

The input signal is taken as Vin (where tr = tf = 2ns, T = 30 ns) and the output is taken at Vout. From Fig. 4a and b the minimum in delay and voltage droop occurs for Co-axial model than that of Cylindrical model. By inserting these RLC model between the tier levels and from Fig. 4c and d the Cylindrical TSV Model has some voltage drop and increase in delay in its output than that of Co-axial TSV Model. Further, increase in (workload) no.of tiers also causes some delay and voltage drop which can be of minimized by changing the parameter values of CTSV gives better results.

The Power analysis by its transient response is based on the electrical performance of a 3-D system. Figure 5 shows the proposed flow model. To understand the implications of power integrity for a 3-D system, we start by investigating a single active tier on a multi-tier system.

CONCLUSION

In this study, Closed-form RLC parameters of TSV was derived from physical parameters and material properties of TSVs and then these electrical parameters of TSV are extracted and the voltage drop is verified using Cadence Virtuoso Schematic. The Power analysis for both cylindrical and co-axial TSV between the circuit RLC model for 2, 3, 4 and 5 tiers were presented in Table 2. Comparing both the structures for different

tiers indicate that the Coaxial TSV Structure have much better crosstalk suppression and power consumption than cylindrical TSV Structure.

REFERENCES

Bermond, C., L. Cadix, A. Farcy, T. Lacrevaz, P. Leduc and B. Flechet, 2009. High frequency characterization and modeling of high density TSV in 3D integrated circuits. Proceeding of IEEE Workshop on Signal Propag on Interconnects, pp: 1-4.

Goldfarb, M.E. and R.A. Pucel, 1991. Modeling via-hole grounds in microstrip. IEEE Microw. Guided W., 1(6): 135-137.

Katti, G., M. Stucchi, K. De Meyer and W. Dehaene, 2010. Electrical modeling and characterization of through silicon via for three-dimensional ICs. IEEE T. Electron Dev., 57(1): 256-262.

Khan, N.H., S.M. Alam and S. Hassoun, 2009. Through-silicon via (TSV)-induced noise characterization and noise mitigation using coaxial TSVs. Proceeding of IEEE International Conference on 3D System Integration (3DIC, 2009), pp: 1-7.

Knickerbocker, J.U., P.S. Andry, B. Dang, R.R. Horton, C.S. Patel, R.J. Polastre, K. Sakuma, E.S. Sprogis, C.K. Tsang, B.C. Webb and S.L. Wright, 2008. 3D silicon integration. Proceeding of 58th Electronic Components and Technology Conference (ECTC, 2008), pp: 538-543.

Liang, F., G. Wang, D. Zhao and B.Z. Wang, 2013. Wideband impedance model for coaxial through-silicon vias in 3-D integration. IEEE T. Electron. Dev., 60(8): 2498-2504.

Rousseau, M., O. Rozeau, G. Cibrario, G. Le Carval, M.A. Jaud, P. Leduc, A. Farcy and A. Marty, 2008. Through-silicon via based 3D IC technology: Electrostatic simulations for design methodology. Proceeding of IMAPS Device Packaging Conference. Pheonix, AZ.

Sparks, T.G., S.M. Alam, R. Chatterjee and S. Rauf, 2006. Method of forming a through-substrate via. U.S. Patent Appl. 20080113505.

Topol, A.W., D.C. La Tulipe, L. Shi, D.J. Frank, K. Bernstein, S.E. Steen, A. Kumar, G.U. Singco, A.M. Young, K.W. Guarini and M. Ieong, 2006. Three-dimensional integrated circuits. IBM J. Res. Dev., 50(4-5): 491-506.

Van Olmen, J., A. Mercha, G. Katti, C. Huyghebaert, J. Van Aelst, E. Seppala, Z. Chao, S. Armini, J. Vaes, R.C. Teixeira, M. Van Cauwenberghe, P. Verdonck, K. Verhemeldonck, A. Jourdain, W. Ruythooren, M. de Potter de ten Broeck, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T.Y. Hoffmann, B. De Wachter, W. Dehaene, M. Stucchi, M. Rakowski, P. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans and B. Swinnen, 2008. 3D stacked IC demonstration using a through silicon via first approach. Proceeding of IEEE International Electron Devices Meeting (IEDM, 2008), pp: 603-606.

Xu, Z. and J.Q. Lu, 2012. Three-dimensional coaxial Through-Silicon-Via (TSV) design. IEEE Electr. Device L., 33(10): 1441-1443.